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Experimental Implementation of Non-binary Cyclic ADCs with Radix Value Estimation Algorithm

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SUMMARY Proof-of-concept cyclic analog-to-digital converters (ADCs) have been designed and fabricated in 90-nm CMOS technology. The measurement results of an experimental prototype demonstrate the effectiveness of the proposed switched-capacitor (SC) architecture to realize a non-binary ADC based on β expansion. Different from the conventional binary ADC, a simple 1-bit/step structure for an SC multiplying digital-to-analog converter (MDAC) is proposed to present residue amplification by β ($1 < \beta < 2$). The redundancy of non-binary ADCs with radix β tolerates the non-linear conversion errors caused by the offsets of comparators, the mismatches of capacitors, and the finite DC gains of amplifiers, which are used in the MDAC. We also employed a radix value estimation algorithm to obtain an effective value of β for non-binary encoding; it can be realized by merely adding a simple conversion sequence and digital circuits. As a result, the power penalty of a high-gain wideband amplifier and the required accuracy of the circuit elements for a high-resolution ADC were largely relaxed so that the circuit design was greatly simplified. The implemented ADC achieves a measured peak signal-to-noise-and-distortion-ratio (SNDR) of 60.44 dB, even with an op-amp with a poor DC gain (< 50 dB) while dissipating 780 μW in analog circuits at 1.4 V and occupying an active area of 0.25×0.26 mm^2.

key words: *Non-binary ADC, Cyclic ADC, Radix value estimation algorithm, β expansion, Multiply-by-β MDAC*

1. Introduction

Mixed-signal LSIs are widely used for data communications, sensor networks, and image processing systems. Their application fields are still expanding significantly. As an interface between the analog world and the digital domain, ADCs should have the attributes of high sampling frequency, high resolution, low cost (coinciding with a small chip area), with low power consumption. CMOS technologies have been developed on the nanometer scale, which has resulted in an amazing increase in the density of LSIs. Digital circuits benefit from not only high density but also high speed and low power in finer CMOS technology. However, the geometric size of analog components is significantly more difficult to match well in a nanometer process; the restriction of the supply voltage limits the dynamic range of analog signals. Furthermore, the degradation of the device characteristics, such as the threshold-voltage mismatch of a transistor pair and the reduction of the drain output resistance r_{ds}, decreases the accuracy of analog circuits. Because each of the above causes CMOS ADC linearity degeneration, robust ADC architecture against device parameter variation is desirable for not only current mixed-signal LSIs but also next-generation CMOS technology.

It is well known that in the conventional binary architecture, the linearity of an ADC is very sensitive to the accuracy of analog components. Therefore, high-accuracy matched components, such as transistors, capacitors, and resistors, and high-gain wideband amplifiers are required to guarantee ADC linearity, which lead to a large chip area and high power consumption. Redundant architectures, such as a non-binary capacitor array structure for SAR ADCs, have been proposed to tolerate the conversion errors caused by incomplete settling [1], [2]; however, high-accuracy matched capacitors are required to guarantee the radix value with high accuracy. A 1.5-bit/stage structure for cyclic/pipeline ADCs also has been proposed to tolerate the conversion errors caused by device non-ideality [3]–[5]; however, high-gain amplifiers are still necessary to satisfy the required ADC linearity. Although digital calibration techniques have been proposed to relax the required performance of the analog elements in pipeline ADCs [6]–[8], the algorithms and their realization circuits are still complex, and calibration time is too long to be used effectively [9]. Consequently, we have proposed a robust ADC architecture based on β expansion, which tolerates the conversion errors caused by the mismatches of capacitors, offsets of comparators and/or amplifiers, and finite gains of amplifiers [10]. Moreover, we proposed a radix value estimation algorithm to obtain the effective radix value for non-binary-to-binary encoding. In a conventional digital calibration technique, the difference between the residue output of $+V_{ref}$ and $-V_{ref}$ is measured and stored as a calibration parameter. However, in our proposed technique, the residue outputs of $+V_{ref}$ and $-V_{ref}$ are measured to calculate the effective radix value. A reliability-enhanced non-binary ADC can be realized just by adding a simple conversion sequence with the effective radix value. As a result, the required higher DC gain of an amplifier and the area penalty of the high-accuracy circuit elements for a high-resolution ADC can be greatly relaxed.

This paper presents a proof-of-concept implementation with switched-capacitor circuits employing a cyclic non-binary ADC architecture with a radix value estimation algorithm. The implemented ADC can achieve an SNDR of 60.44 dB using an op-amp with a DC gain of approximately 47 dB. The measured results of the implemented chip show that the above robust architecture and algorithm are effec-

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tive.

2. Non-binary Cyclic ADC Architecture

Figure 1 shows a simplified block diagram of the proposed non-binary cyclic ADC based on β expansion. The conversion stage contains a 1-bit sub-ADC (comparator), a 1-bit digital-to-analog converter (DAC), an analog subtractor, and a multiply-by-β gain amplifier. This conversion stage resolves one bit and feeds back the residual signal to the input node for the next conversion step. The re-sampled residual is processed incrementally to realize a high-resolution conversion. The proposed ADC architecture is similar to the conventional binary cyclic ADC structure; however, a multiply-by-β ($1 < \beta < 2$) amplifier is used instead of using a gain-of-2 amplifier; simultaneously, the output of the DAC is scaled by $\beta - 1$.

As shown in Fig. 2(a), while we assume that the analog input signal is in the range of $[-V_{ref}, V_{ref}]$, the threshold voltage of the comparator is 0 V, the output code of a sub-ADC in the *Nth* step is b_N ($b_N = 0$ or 1), and the corresponding output voltage of the 1-bit DAC is 0 or V_{FS} (the full-scale voltage of the analog input signal, $V_{FS} = 2V_{ref}$). Then, the residue of the 1st, 2nd, and 3rd conversion steps is expressed as

$$V_{res1} = \beta V_{in} - b_1(\beta - 1)V_{FS} \quad (1)$$

$$\begin{aligned} V_{res2} &= \beta V_{res1} - b_2(\beta - 1)V_{FS} \\ &= \beta[\beta V_{in} - b_1(\beta - 1)V_{FS}] - b_2(\beta - 1)V_{FS} \end{aligned} \quad (2)$$

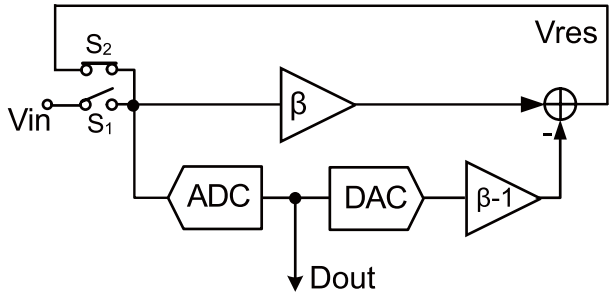

Fig. 1 Simplified block diagram of the non-binary cyclic ADC based on β expansion.

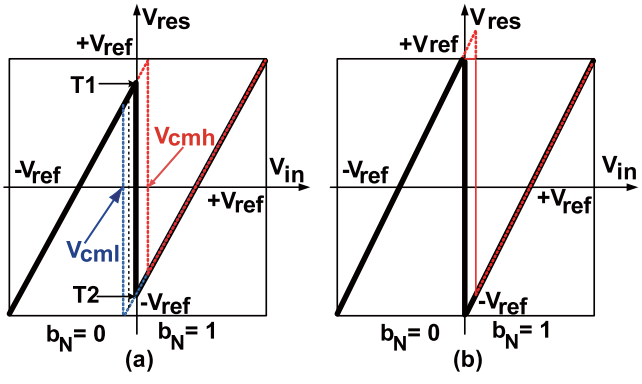

Fig. 2 Transfer characteristic of the conversion stage. (a) radix = $\beta < 2$. (b) radix = 2.

$$\begin{aligned} V_{res3} &= \beta V_{res2} - b_3(\beta - 1)V_{FS} \\ &= \beta\{\beta[\beta V_{in} - b_1(\beta - 1)V_{FS}] \\ &\quad - b_2(\beta - 1)V_{FS}\} - b_3(\beta - 1)V_{FS}. \end{aligned} \quad (3)$$

Equation (3) also is written as

$$V_{res3} = \beta^3 V_{in} - (\beta - 1)(\beta^2 b_1 + \beta^1 b_2 + \beta^0 b_3)V_{FS}. \quad (4)$$

By dividing by $\beta^3 V_{FS}$, Eq. (4) is expressed as

$$\frac{V_{in}}{V_{FS}} = (\beta - 1)\left(\frac{b_1}{\beta} + \frac{b_2}{\beta^2} + \frac{b_3}{\beta^3}\right) - \frac{1}{\beta^3}\frac{V_{res3}}{V_{FS}}. \quad (5)$$

Thus, for a cyclic ADC with N steps, we have

$$\frac{V_{in}}{V_{FS}} = (\beta - 1)\sum_{n=1}^{N}\frac{1}{\beta^n}b_n - \frac{1}{\beta^N}\frac{V_{resN}}{V_{FS}}. \quad (6)$$

Equation (6) implies that the ratio of the analog input V_{in} to V_{FS} can be expressed as a digital code series of Dout = $[b_1, b_2, ..., b_{N-1}, b_N]$ (the output codes of N-step ADC) with quantization error. At the same time, we call the following mapping equation the β expansion of an analog signal (β is a non-integer number as the radix of the ADC).

$$\frac{V_{in}}{V_{FS}} = (\beta - 1)\sum_{n=1}^{N}\frac{1}{\beta^n}b_n. \quad (7)$$

In the case of $\beta = 2$, the β expansion expressed as Eq. (7) can be simplified to a binary expansion as follows:

$$\frac{V_{in}}{V_{FS}} = \sum_{n=1}^{N}\frac{1}{2^n}b_n. \quad (8)$$

Then, the cyclic ADC operation is performed in a binary format. Alternatively, in the case of $1 < \beta < 2$, the ADC operation is performed in a non-binary format. In the 1-bit/step cyclic ADC with a stage gain of two, any non-ideality such as a comparator/amplifier offset, the inter-stage gain error caused by the mismatch of capacitors and/or finite gain of an amplifier will damage the linearity of the ADC [12]. Figure 2(b) shows the transfer function of the conversion stage while $\beta = 2$. The solid line shows the ideal characteristic, and the dotted line shows the characteristic with a comparator offset. It is obvious that the over-ranged residue of the conversion stage will cause the error code at the output of the ADC. On the other hand, Fig. 2(a) shows the transfer function of the conversion stage while $1 < \beta < 2$. We can see that the residue is still in the allowed input range for the next conversion step, even when a comparator with an offset is used.

The second term on the right side of Eq. (6) is the residue of the last step of the conversion, and this residue is considered to be the quantization error of the ADC. In the non-binary ADC, because $\beta < 2$, we know that $1/2^N < 1/\beta^N$. This implies that the effective conversion resolution/step of a non-binary cyclic ADC with radix $\beta < 2$ is less than that of a binary ADC. Therefore, we see that while

the non-binary cyclic ADC with the radix value of $1 < \beta < 2$ is applied, more conversion steps are necessary to satisfy the required resolution of the binary ADC. Normally, to realize a binary ADC with N-bit resolution, the required conversion step number M of the non-binary ADC must satisfy the formula of $1/\beta^M < 1/2^N$ [13], [14]. In our implementation, the ADC operates at 20 steps/sample and outputs a 20-bit digital code for one conversion. However, we only use the 12-bit non-binary output code to satisfy the 10-bit resolution of a binary ADC when $\beta \simeq 1.8$. The redundancy of a non-binary ADC relaxed the required accuracy of analog circuit components, and the robustness of a non-binary ADC tolerates not only the offset of a comparator and/or amplifier but also the inaccurate gain of the conversion stage.

3. Multiply-by-β Conversion Stage

Figure 3 shows the SC implementation of the conversion stage for the proposed non-binary ADC. Although a single-ended configuration is shown for simplicity, the actual implementation is fully differential. Normally, the combination of a multiply-by-β amplifier and DAC is called a multiplying DAC (MDAC). The operation of a simplified multiply-by-β amplifier is illustrated in Fig. 4. During the sampling phase shown in Fig. 4(a), the analog input V_{in} is sampled by the capacitors C_s and C_f. During the amplifying phase shown in Fig. 4(b), C_f is connected to the output of the amplifier V_{res}, and C_s is connected to the reference voltage of $+V_{ref}$ or $-V_{ref}$, depending on the output code of sub-ADC b_N. Assuming that the DC gain of the amplifier is infinite, according to the charge conservation law, the residue of the conversion stage is expressed as

$$V_{res} = \frac{C_s + C_f}{C_f} V_{in} - b_N \frac{C_s}{C_f} V_{FS}. \tag{9}$$

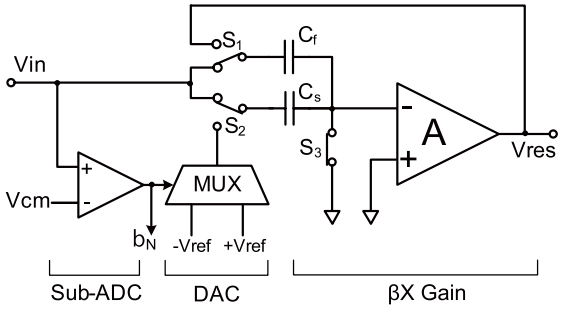

Fig. 3 Switched-capacitor implementation of conversion stage.

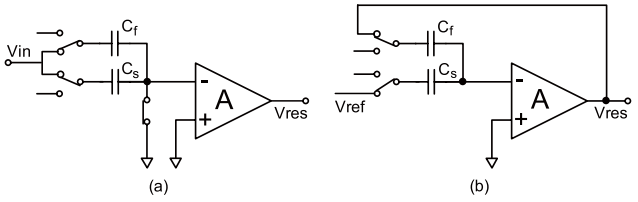

Fig. 4 Switched-capacitor multiply-by-β amplifier. (a) Sampling phase. (b) Amplifying phase.

Here, $b_N = 0$ or 1 and $V_{FS} = 2V_{ref}$. Actually, this multiply-by-β SC circuit is the same as the conventional multiply-by-2 MDAC in the case of $C_s = C_f$; however, although we designed the capacitors as $C_s = (\beta - 1)C_f$, the residue is expressed as

$$V_{res} = \beta V_{in} - b_N(\beta - 1)V_{FS}. \tag{10}$$

Equation (10) shows that multiply-by-β amplification is realized simply only by changing the ratio of capacitors in a conventional MDAC. In our implementation, $C_s = 0.25$ pF, and the capacitor ratio is designed as $C_s/C_f = 5/6$ to allow a simple capacitor layout design. As explained later, in our proposed ADC architecture, neither accurate matching of capacitors nor high-gain amplification is required because the uncertain stage gain of the conversion stage can be estimated. We just use this simple multiply-by-β structure to obtain the digital output code for β encoding and amplify the residue for the next conversion step.

4. Radix Value Estimation Algorithm

In the binary 1-bit/step cyclic ADC structure with a stage gain of two, the encoding is simple because the radix value of the output code is considered to be two. However, any non-ideality, such as comparator offset, capacitor mismatch, or a finite gain amplifier, will damage the linearity of the ADC [12]. In our proposed non-binary ADC architecture, the stage gain is less than two, and the redundancy tolerates the above non-idealities so that the ADC output can be kept linear by β-encoding the output code with Eq. (7). However, the β encoding according to Eq. (7) is impractical without a certain radix value of β. The key point of a non-binary ADC is encoding the output code with an accurate radix value to guarantee the linearity of the ADC. Theoretically, the value of β can be designed by the ratio of capacitors, but the capacitor mismatch will cause random variation in the radix value. Moreover, the finite gain of the amplifier causes stage gain degeneration. Assuming that the finite DC gain of the amplifier is A_0, then the residue of the conversion stage can be expressed as

$$\begin{aligned} V_{res} &= \frac{A_0}{1 + \frac{C_s}{C_f} + A_0} \left(\frac{C_s + C_f}{C_f} V_{in} - b_N \frac{C_s}{C_f} V_{FS} \right) \\ &= \frac{A_0}{\beta + A_0} \left(\beta V_{in} - b_N(\beta - 1)V_{FS} \right) \qquad (11) \\ &= \beta_{eff} V_{in} - b_N(\beta_{eff} - 1)hV_{FS}. \qquad (12) \end{aligned}$$

Here, $\beta_{eff} = k\beta$, $h = k(\beta - 1)/(k\beta - 1)$, and $k = A_0/(\beta + A_0)$. It is clear that not only capacitor mismatch but also the finite gain of an amplifier have direct influences on the value of β. However, the ADC output remains linear in the case of the β encoding with an effective stage gain of β_{eff}. Therefore, we proposed a radix value estimation algorithm to obtain an effective radix value of β_{eff} for non-binary encoding to satisfy the required linearity of the ADC [10], [11]. The estimation technique can be realized simply with the utilization of

redundancy in a non-binary ADC.

As shown in Fig. 2(a), while we shorten the differential input nodes of the ADC (that is, the input signal is around the analog common level), and run AD conversion after we preset the input of the DAC as 0 or 1, then we can obtain two digital codes:

$$D_{out-m0} = [0, b_{02}, ..., b_{0N-1}, b_{0N}] \ (b_{01} = 0), \quad (13)$$

$$D_{out-m1} = [1, b_{12}, ..., b_{1N-1}, b_{1N}] \ (b_{11} = 1), \quad (14)$$

which correspond to the residue signals of T1 and T2 in Fig. 2(a), respectively. In a binary ADC, the output codes of D_{out-m0} and D_{out-m1} indicate different analog input values. However, in a non-binary ADC, redundant digital D_{out-m0} and D_{out-m1} indicate the same analog input despite the offset voltage of the comparator. Because one analog input level of V_{in} can be expressed by two digital codes as

$$V_{in} = D_{out-m0} = D_{out-m1} \quad (15)$$

$$= \sum_{n=1}^{N} \beta^{n-1} b_{0n} = \sum_{n=1}^{N} \beta^{n-1} b_{1n}, \quad (16)$$

then the solution of β for Eq. (16) is the effective radix value of the non-binary ADC. For example, T1 and T2 are converted to 5-bit digital codes as follows:

$$T1(Analog) \Leftrightarrow D_{out-m0}(Digital) = [0, 1, 1, 1, 0],$$

$$T2(Analog) \Leftrightarrow D_{out-m1}(Digital) = [1, 0, 0, 0, 1].$$

In a binary ADC, $D_{out-m0} = 14$ and $D_{out-m1} = 17$, which indicate different analog input values. On the other hand, when we substitute D_{out-m0} and D_{out-m1} into Eqs. (15) and (16), then we obtain:

$$V_{in} = D_{out-m0} = D_{out-m1} \quad (17)$$

$$= \beta^3 + \beta^2 + \beta^1 = \beta^4 + \beta^0. \quad (18)$$

The solution of β for Eq. (18) is $\beta = 1.772$. This result implies that an unknown value of β (as the same of radix value of the ADC) can be calculated from the above digital codes of D_{out-m0} and D_{out-m1}.

Although it is too difficult to resolve a high-order equation of β from Eq. (16) for a high-resolution ADC, we can calculate the difference between the two digital codes of D_{out-m0} and D_{out-m0} easily. Then, the error between the digital codes of D_{out-m0} and D_{out-m0} is expressed as

$$e(\beta) = \sum_{n=1}^{N} \beta^{n-1}(b_{0n} - b_{1n}). \quad (19)$$

According to our simulation results, $e(\beta)$ is the monotonic function of β in the range of $1.5 < \beta < 2$. Therefore, when we sweep the value of β, the effective radix value of β_{eff} can be obtained when $|e(\beta)|$ is nearest to 0. As a result, the non-linear errors caused by capacitor mismatch and the finite gain of the amplifier can be resolved overall while encoding the output code as Eq. (7) with the estimated effective radix value.

Our proposed algorithm is a foreground technique to estimate the effective radix value for a non-binary cyclic ADC. It is effective for the variation of the process, voltage, and temperature when this estimation function is carried out before AD conversion. The foreground calibration is very popular for a high-resolution ADC either with an analog technique [15] or in the digital domain [7], and both of them need an additional DC voltage in the calibration process. In our proposed effective radix value techniques, we also assumed that the analog input of a common level signal should be used; however, no additional DC voltage is required at all. When the estimation function is carried out, the differential input nodes of the ADC are shortened so that the input of the ADC is equivalent to the analog common level for the estimation process.

5. Circuit Implementation

The proposed cyclic ADC was designed and fabricated with a 1P9M 90-nm CMOS technology without any option for precision capacitors and low-threshold voltages. Gate-boosted NMOS sampling switches were used at the input of the ADC to avoid the nonlinear effect from the switch-ON resistance [16], whereas all the others are CMOS switches. Hence, because the proposed architecture tolerates a poor gain amplifier, the single-stage folded-cascode amplifier shown in Fig. 5 is designed for our ADC, and the simulated result of the DC gain is 47.6 dB at $V_{dd} = 1.4$ V. A latched comparator without any input offset cancellation shown in Fig. 6 is used as the sub-ADC [17]. Non-overlapping clocks are used to avoid charge loss by sampling switches. A clock generator circuit and cyclic control logic circuits also are designed and implemented on the chip. The digital circuits operate at 1.2 V. Because we aim at proving the validity of

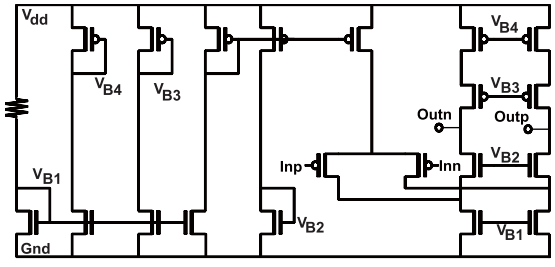

Fig. 5 Schematic of a single-stage folded-cascode amplifier.

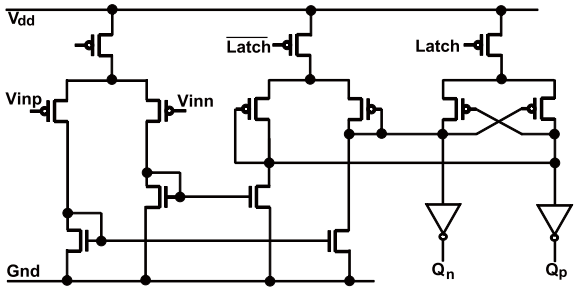

Fig. 6 Schematic of latched comparator.

the proposed architecture and radix estimation algorithm, we did not optimize the op-amp and comparator or optimize for low power consumption.

The capacitors in the MDAC were chosen as C_s = 250 fF and $C_f = 6C_s/5$ = 300 fF to satisfy the required thermal noise for 10-bit resolution. To verify the robustness to capacitance mismatches with our radix estimation algorithm, we designed and fabricated two ADCs (chip A and chip B) with the same circuit elements, including amplifiers, SWs, comparators, clock generator circuits, and logic circuits, except for the layout of the capacitors in the MDAC. In chip A, the capacitors were realized using multiple unit-capacitor cells for designing the capacitor ratio as C_s/C_f = 5/6. A unit-capacitor cell was realized with an MIM structure for high-capacitance density in a small chip area. On the other hand, in chip B, the capacitor ratio of C_s/C_f = 5/6 is realized only by the simple area ratio of the two capacitors without a unit-capacitor cell. Figure 7 shows a microphotograph of chip A and the layout of the ADC, and Fig. 8 shows that of chip-B. The active core size of the ADC in chip A is $245 \times 260\,\mu m^2$, and the core size of the ADC in chip B is $225 \times 220\,\mu m^2$. The capacitances of C_s and C_f in chip B are the same as those in chip A; however, the occupied area is 1/6 that in chip A.

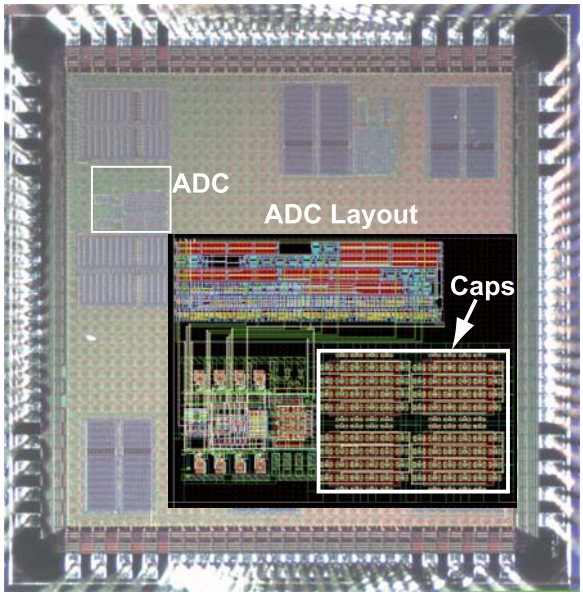

Fig. 7 Chip A micrograph and layout.

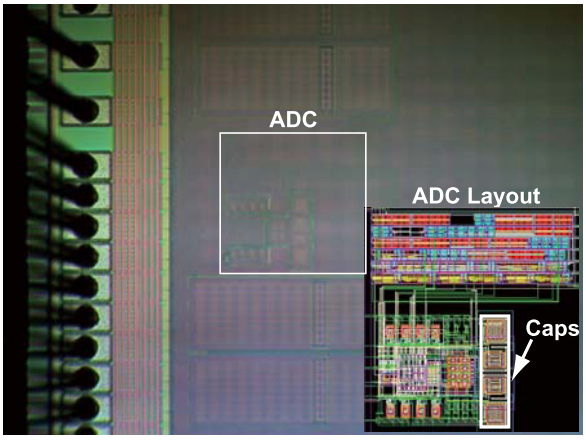

Fig. 8 Chip B micrograph and layout.

6. Experimental Results

The prototype of the proposed 10-bits ADC is fabricated with a radix value estimation mode and an operation mode. After powering on the ADC, it is first set to the foreground estimation mode. In this mode, the differential inputs of the ADC were shortened, and AD conversion was performed. In each conversion operation, the first step digital input for the switch of the MDAC (the same as the MSB of the digital output code of the ADC) was settled to $+V_{ref}$ and $-V_{ref}$ (shown in Fig. 3) alternately. Therefore, we can obtain two ADC output digital codes corresponding to the same analog input (analog common level), but the MSB of the ADC outputs code varies between 1 and 0 alternately as well. These two digital output codes are considered as D_{m0} and D_{m1} in Eq. (19), then we sweep the value of β from 1.800 to 1.833 (the radix value designed by the capacitor ratio of $1+C_s/C_f$) with a step of 1/1000 to meet the effective radix value of β_{eff} when $|e(\beta)|$ is nearest to 0. The radix value calculated according to the explained algorithm in Sect. 4 was computed with 64 averages by an off-chip computer. Certainly, the radix value estimation can be realized with logic circuits, and some overhead must be paid for the chip area and power; however, digital circuits can be shrunk significantly more than analog circuits in current technology. Figure 9 shows the value of $e(\beta)$ calculated with the results of chip A according to Eq. (19) while we swept the value of β. The zero crossing point of $e(\beta)$ was searched for, which resulted in the effective β of ADC in chip A as β_{effA} = 1.8131.

In the operation mode, the output of the ADC was encoded according to Eq. (7) with the above estimated β_{effA} corresponding to analog inputs. Figure 10 shows the measured output power spectrum of the ADC in chip A with the above effective value of β. The peak SNDR was

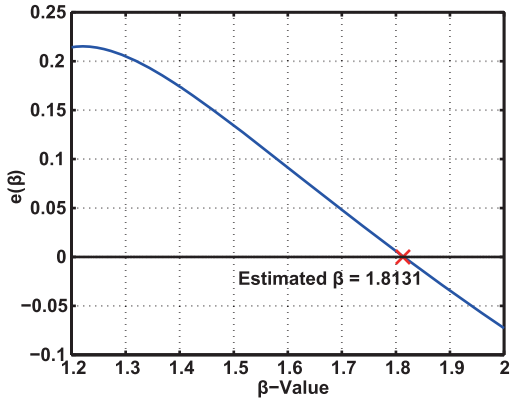

Fig. 9 β estimation error of chip A.

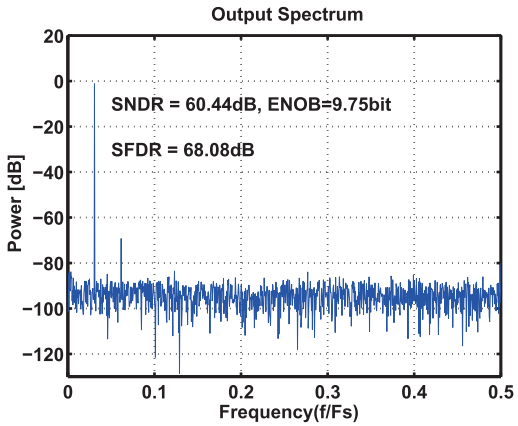

Fig. 10 Output power spectrum of cyclic ADC in chip A with estimated value of β.

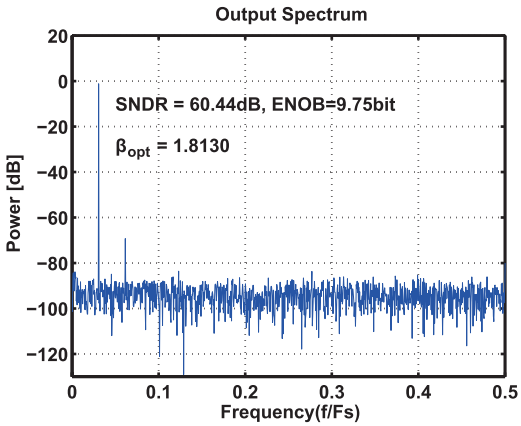

Fig. 12 Output power spectrum of cyclic ADC in chip A with optimum β.

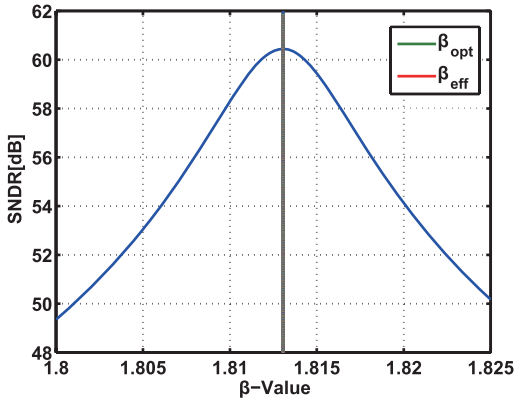

Fig. 11 SNDR of ADC vs. β estimation of chip A.

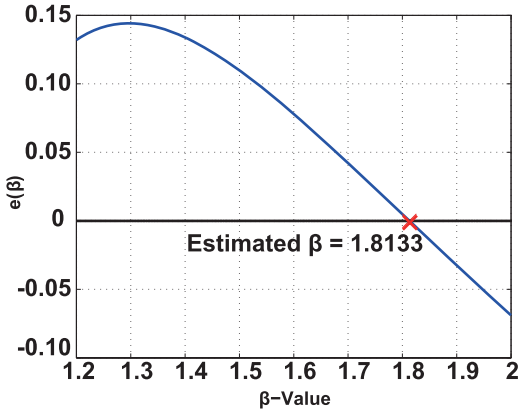

Fig. 13 β estimation error of chip B.

60.44 dB while a sinusoid differential input of 30.2 kHz with 0.9 Vpp was sampled at 1 MS/s with a power consumption of 780 μW. The second-order harmonic distortion was produced by the layout mismatch between the differential analog input pair.

To verify the effectiveness of the proposed radix value technique, we also calculated the SNDR with the same output codes of chip A while we swept the value of β. The results of the study of SNDR vs. β are shown in Fig. 11. We see that a maximum SNDR = 60.44 dB was achieved when β was 1.8130, and we call this optimum value β_{optA} = 1.8130. From the above comparison, we see that the effective β (β_{effA} = 1.8131) estimation accuracy was less then 0.006% with our proposed technique. Figure 12 shows the measured output power spectrum for the same output codes of a sinusoidal input with optimum β of chip A. We find that the SNDR is the same as the measured SNDR of 60.44 dB.

We also measured chip B with the same method as that for chip A. Figure 13 shows $e(\beta)$ calculated with the results of chip B according to Eq. (19) while we swept the value of β. Then, we found that the effective value of β of the ADC in chip B was β_{effB} = 1.8133. Figure 14 shows the measured output power spectrum of the ADC in chip B with β_{effB} = 1.8133; we see that a peak SNDR of 60.39 dB is

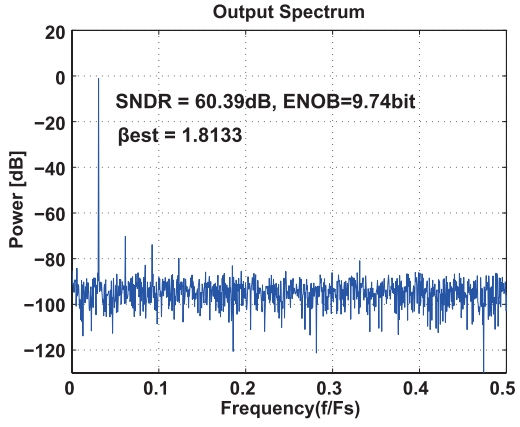

Fig. 14 Output power spectrum of cyclic ADC in chip B with estimated β.

achieved. Here, the third-order harmonic distortion was produced by the non-linearity of the operational amplifier, and the second-order and fourth-order harmonic distortions were produced by the mismatch between the differential analog input pair as mentioned before. From the previous measurement results, we confirmed that the resolution of chip B was almost the same as chip A, even though small-area capacitors with greater mismatches were used.

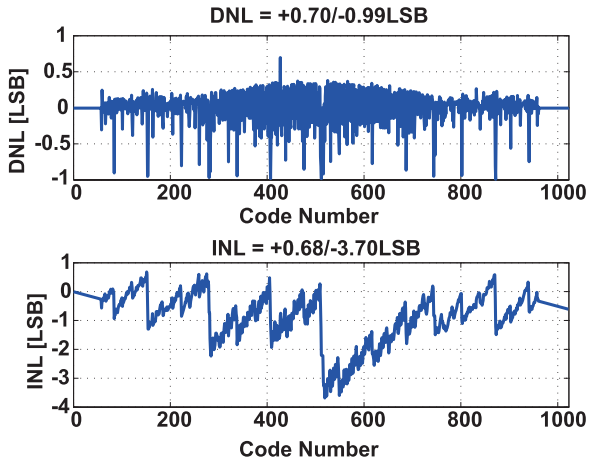

Fig. 15 Measured DNL and INL with designed radix value of chip B.

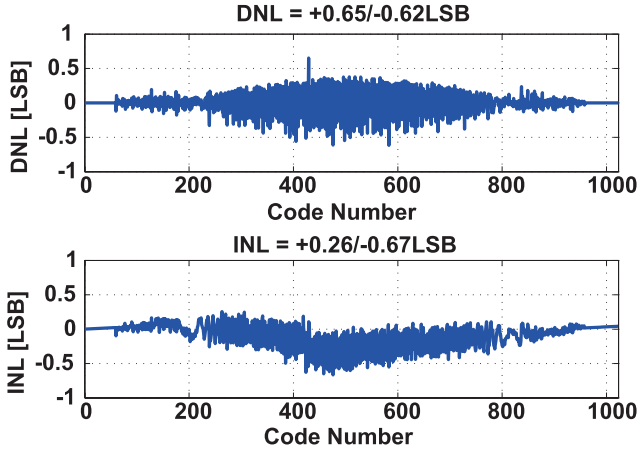

Fig. 16 Measured DNL and INL with estimated radix value of chip B.

Table 1 Performance summary and comparison.

	Proposed Design (Chip B)	[18]JSSC
Technology (nm)	90	90
Vdd (V)	1.4	1
Sampling Rate (MS/s)	1	50
Resolution (bits)	10	9
DNL (LSB)	0.65/−0.62	0.43/−0.47
INL (LSB)	0.26/−0.67	0.63/−0.60
ENOB (bit)	9.75	8.10
SNDR (dB)	60.39	50.5
Chip area (mm^2)	0.049	0.019
Power (mW)	0.780	6.9

Figure 15 shows the measured DNL/INL of chip B with the designed radix value of $Radix = (C_s + C_f)/C_f$. The DNL is 0.70/−0.99LSB and the INL is 0.68/−3.70LSB. Figure 16 shows the measured DNL/INL of chip B with the estimated radix value. The DNL is 0.65/−0.62LSB, and the INL is 0.26/−0.67LSB. It is obvious that the DC characteristic of the ADC is improved with the estimated effective radix value.

The performance of the proposed ADC (chip B) and measurement results comparison is summarized in Table 1. These measurement results show that by using our proposed architecture and radix value estimation algorithm, not only the required DC gain op-amp, but also the required matching accuracy of capacitors for the high-resolution ADC can be largely relaxed. Our approach is suitable for current finer CMOS technologies.

7. Conclusion

We have designed and fabricated non-binary cyclic ADCs based on β expansion with a radix value estimation algorithm in 90-nm CMOS technology. The redundancy of the proposed ADC tolerates the conversion errors caused by coarse-accuracy devices and circuit components so that the circuit design can be greatly simplified. Measurement results demonstrate the validity of the proposed ADC architecture and the effectiveness of the proposed radix value estimation algorithm.

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