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Robust Cyclic ADC Architecture Based on β-Expansion

Rie SUZUKI[†], ***Member***, **Tsubasa MARUYAMA**[†], ***Nonmember***, **Hao SAN**[†a)], ***Member***, **Kazuyuki AIHARA**[††], ***and*** **Masao HOTTA**[†], ***Fellows***

SUMMARY In this paper, a robust cyclic ADC architecture with β-encoder is proposed and circuit scheme using switched-capacitor (SC) circuit is introduced. Different from the conventional binary ADC, the redundancy of proposed cyclic ADC outputs β-expansion code and has an advantage of error correction. This feature makes ADC robust against the offset of comparator capacitor mismatch and finite DC gain of amplifier in multiplying-DAC (MDAC). Because the power penalty of high-gain wideband amplifier and the required accuracy of circuit elements for high resolution ADC can be relaxed, the proposed architecture is suitable for deep submicron CMOS technologies beyond 90 nm. We also propose a β-value estimation algorithm to realize high accuracy ADC based on β-expansion. The simulation results show the effectiveness of proposed architecture and robustness of β-encoder.

key words: *robust ADC, β-expansion, redundancy, cyclic ADC, radix-value estimation algorithm*

1. Introduction

Mixed-signal LSIs are widely used for communications, sensor networks and image processing systems. As an interface between the analog world and the digital domain, the analog-to-digital converters (ADCs) are desired with the performances of high resolution, high sampling frequency, low cost (the same word as small chip area) with low power consumption. Digital circuits benefit from high density, high speed and low power consumption as well as CMOS process be shrunk into nanometer scale according to ITRS load map [1]. On the other hand, geometric size of analog components is much more difficult to be matched well; the restriction of supply voltage for nanometer process limits the dynamic range of signals. Furthermore, the device characteristics degradation such as threshold voltage mismatch of transistor pair and reduction of drain output resistance rds damage the accuracy of analog circuits. Because each of above causes the CMOS ADC performance degeneration, the robust ADC architecture is desirable for not only nowadays mixed signal LSIs but also next generation CMOS technology.

It is well known that in the conventional binary architecture, the linearity of ADC is very sensitive to the accuracy of analog components. Therefore, high accuracy matched devices, such as transistors, capacitors and resistors, high gain wide bandwidth amplifiers are necessary to satisfy the required ADC linearity, which cause large chip area and high power consumption.

Cyclic and pipeline ADC architectures with redundant bit have been proposed to reduce the sensitivity against component non-idealities (ex. amplifier/comparator offset). As proposed in [2], cyclic ADC has one redundant bit at backend sub-ADC, so that the influence of offset error of amplifier and comparator can be cancelled by digital correction technique with the redundant bit. Pipeline ADC with 1.5 bit/stage architecture has been reported in [3], and the error correction using the redundant bit at each pipelined stage becomes the most popular technique for pipeline ADCs. However, either cyclic or pipeline ADC with redundant bit still requires high DC gain of amplifier and high accuracy capacitor ratio to ensure the residue signal be amplified by 2 with high accuracy. In deep submicron CMOS technologies beyond 90 nm, it is difficult to achieve either high accuracy capacitor ratio or high DC gain of amplifier. Digital calibration techniques [4] have been proposed to overcome the above problems. However, the algorithms' and circuits' control logics are still complex and calibration time is too long to be used effectively. Then we proposed a robust ADC structure based on β-expansion [5], which provides conversion technique in non-binary manner [6]–[8]. The redundancy of non-binary ADC relaxes the requirement for circuit components such as the offset of amplifier and/or comparator, mismatch of capacitors and/or current cells.

In this paper, we present an AD conversion stage with switched-capacitor MDAC to realize a β-expansion based 1 bit/step cyclic ADC. We also propose β-estimation algorithm to get the right radix value of ADC, there is not any digital calibration technique is required. Moreover, circuit scheme of switched-capacitor cyclic ADC based on β-expansion is discussed. Simulation results show that above robust architecture and algorithm are effective.

2. β-Expasion Based ADC

2.1 β-Expasion Based Cyclic ADC Architecture

The Cyclic ADC conversion stage contains a 1 bit sub-ADC, a 1 bit digital-to-analog converter (DAC), an analog subtractor, and a gain amplifier [2]. This conversion stage resolves one bit and feedbacks the residual signal to the input node of

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[†]The authors are with Tokyo City University, Tokyo, 158-8557 Japan.
[††]The author is with Institute of Industrial Science, The University of Tokyo, Tokyo, 153-8505 Japan.
a) E-mail: hsan@tcu.ac.jp

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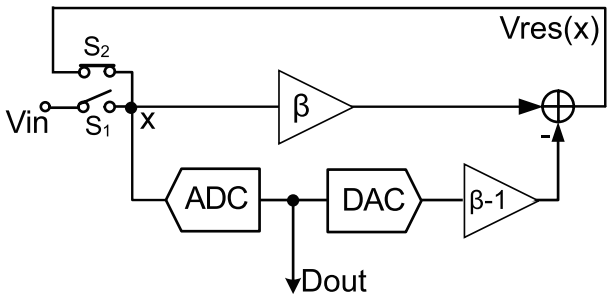


Fig. 1 Simplified block diagram of the cyclic ADC based on β-expansion.

conversion stage again for next conversion step. Normally, the analog input signal V_{in} $(0 < x < 1)$ is expressed as

$$V_{in} = \sum_{i=1}^{\infty} b_i \, 2^{-i} \tag{1}$$

The output code of sub-ADC for the *ith*-step is b_i ($b_i = 0$ or 1) and radix is 2.

According to β-expansion [6], the block diagram of β-expansion-based conversion stage is shown in Fig. 1. The analog input x also can be expressed as

$$V_{in} = \sum_{i=1}^{\infty} (\beta - 1) b_i \, \beta^{-i} \tag{2}$$

The output code b_i is 0 or 1, too; however, the radix is β which maybe any value in the range of $1 < \beta \leq 2$. The term of $(\beta - 1)$ is a normalization factor to keep the full-scale of conversion result being 1. We also call this encode technique based on β-expansion as β-encoding.

The operation of β-expansion-based ADC can be considered as a pipeline or cyclic ADC. The analog signal is resolved 1 bit with the sub-ADC at each stage, then the output of DAC is subtracted from amplified-by-β analog input to get residual output. The resolution of ADC depends on the number of conversion steps. High resolution can be obtained by cascading the AD conversion stage in pipeline manner or using the same conversion stage in cyclic method. The transfer function of residue value $V_{res}(x)$ can be expressed as:

$$V_{res}(x) = \begin{cases} \beta x & b_i = 0 \;\; (x < \upsilon) \\ \beta x - (\beta - 1) & b_i = 1 \;\; (x \geq \upsilon) \end{cases} \tag{3}$$

Here, β is the stage gain of the conversion stage and υ is threshold voltage of sub-ADC. Figure 2 shows the β-map of β-expansion-based ADC [5]. Because the radix of β-expansion-based ADC is less than that of binary ADC, more conversion steps (the same as bit numbers) are necessary to achieve the equivalent resolution of binary ADC. Normally, the accuracy of binary ADC is evaluated by referring quantization error. However, for a non-binary ADC, we have to consider not only quantization error but also truncation error for a fractional radix. While the resolution (bit number) of binary ADC is N, radix value of non-binary ADC is β, then

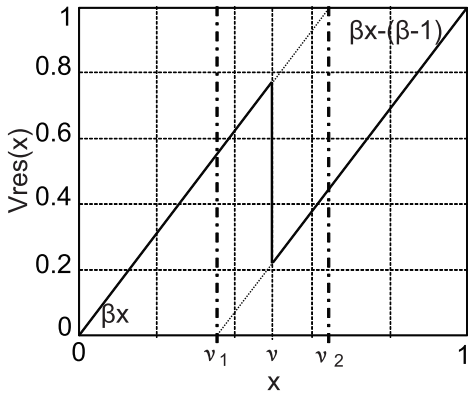


Fig. 2 β-map of β-expansion-based ADC.

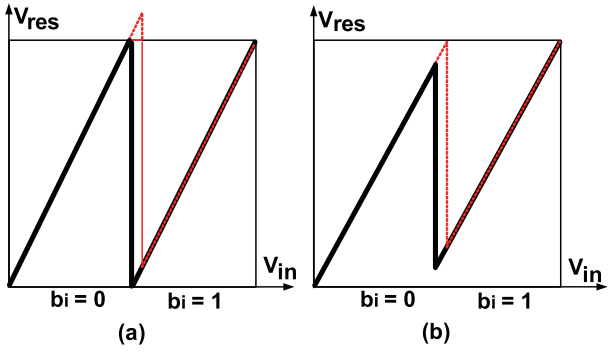


Fig. 3 Transfer characteristic of the conversion stage. (a) radix = 2. (b) radix = $\beta < 2$.

required conversion steps (bit number) of non-binary ADC L can be expressed as the following [9]:

$$L > \frac{N+1}{\log_2 \beta}. \tag{4}$$

2.2 Redundancy in Cyclic ADC Using β-Encoding

It is well known that in a binary cyclic/pipeline ADC with the inter-stage gain of 2, any non-ideal characteristics such as reference voltage variation or gain error will damage the linearity of ADC. As shown in Fig. 3(a), the deviation of comparator threshold voltage causes the signal losses of residue, and then causes the miss code at the output of ADC. On the other hand, in a non-binary ADC with stage gain of β, as shown in Fig. 3(b), since $\beta < 2$, the redundancy at residue tolerates deviation of threshold voltage or gain error. It should be noted that in a non-binary ADC, the reference voltage of sub-ADC is not necessary at the center of full-scale. It can be any value in the range of $\nu_1 < \nu < \nu_2$ as shown in Fig. 2. Here ν_1 and ν_2 are defined as:

$$\nu_1 = 1 - \frac{1}{\beta}, \qquad \nu_2 = \frac{1}{\beta}. \tag{5}$$

As shown in Fig. 4, either the deviation of comparator threshold voltage or DC offset at input nodes of amplifier

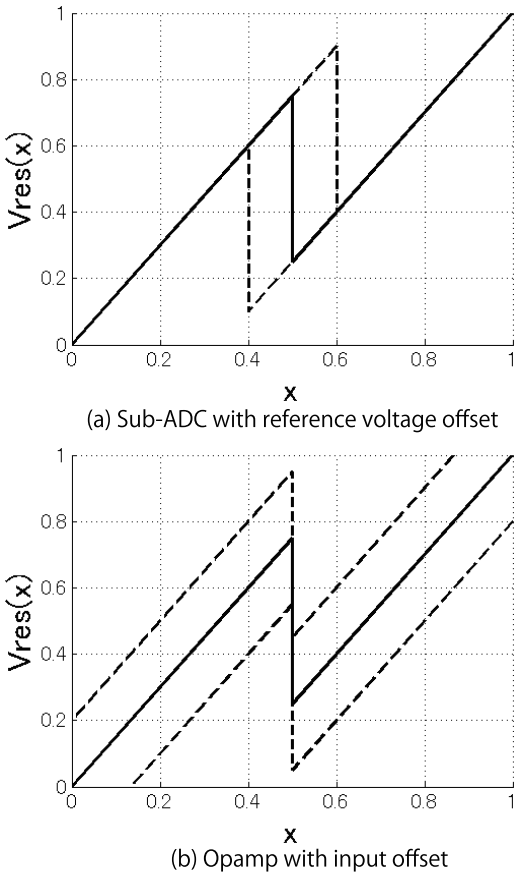


Fig. 4 Transfer characteristic of β-expansion-based ADC with non-ideal offset.

will cause transfer curve shift from the ideal characteristic. However, with the redundancy in the transfer curve, the residue signal still in the allowable input range for the next AD conversion stage. It means that in a non-binary ADC, although the non-ideal factors could cause the transfer curve shift, the output of ADC is still kept linear with the error correcting function according to β-encoding. The 1.5 bit/stage architecture with 3-level sub-ADC has been proposed to tolerate the offset voltage at the conversion stage [3]. The redundancy of each stage keeps the output linearity even with non-ideal comparator. However, 3-level ADC needs 2 reference voltages and 2 comparators, thus the circuits are complex and dissipate more power. β-encoding provides error correction technique to tolerate the non-ideal factors in ADC, however, there are some problems to be resolved to realize non-binary ADC. (1) How we can realize the conversion stage shown in Fig. 1 to get the residual signal with multiply-by-β MDAC. (2) How we can get the right value of β to realize the β-encoding of Eq. (2).

To answer these problems, we propose a MDAC architecture with inter-stage gain being $1< \beta \leq 2$ and a β-value estimation algorithm to realize a cyclic β-expansion-based ADC.

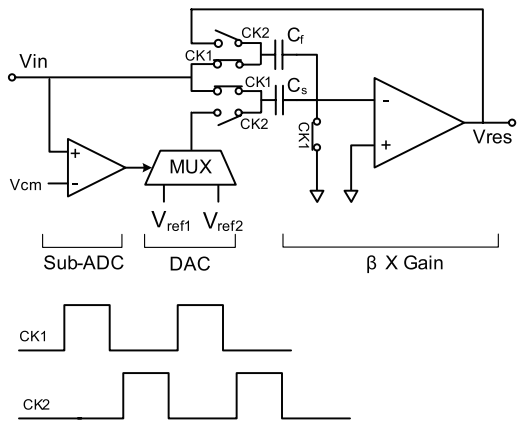


Fig. 5 Switched-capacitor implementation of conversion stage.

3. Proposed Conversion Stage Architecture

3.1 Conversion Stage for β-Encoding

Figure 5 shows switched-capacitor (SC) implementation of conversion stage for proposed cyclic ADC. Although a single-ended configuration is shown for simplicity, the actual implementation is fully differential. According to the charge conservation law, and assuming that the DC gain of amplifier is infinite, then the residue of conversion stage is expressed as

$$V_{res} = \frac{C_s + C_f}{C_f} V_{in} - b_i \frac{C_s}{C_f} V_{ref}. \tag{6}$$

In conventional binary ADC, capacitors C_s and C_f are nominally equal to realize multiply-by-2 amplification. At the same time, high accurate matched capacitors and high DC gain amplifier are necessary to keep the linearity of ADC. On the other hand, in our proposed architecture, we just modify the ratio of two capacitors C_s and C_f as

$$C_s/C_f = (\beta - 1)/1. \tag{7}$$

Therefore, Eq. (6) also can be expressed as

$$V_{res} = \beta V_{in} - b_i(\beta - 1)V_{ref}. \tag{8}$$

to realize multiply-by-β amplification to satisfy the transfer function in Eq. (vresx). It should be noted that in the proposed multiply-by-β MDAC, neither high accurate matched capacitors nor high DC gain amplifier is required. The mismatch between two capacitors should cause the variation of β-value. While the finite DC gain of op-amp is A, then the residue of conversion stage should be expressed as

$$\begin{aligned} V_{res} &= \frac{\beta}{1 + \dfrac{\beta}{A}} \left(\beta V_{in} - b_i(\beta - 1)V_{ref}\right) \\ &= \beta_{eff} V_{in} - b_i(\beta_{eff} - 1)hV_{ref}, \end{aligned} \tag{9}$$

here, β_{eff}=$k\beta$, h=$k(\beta-1)/(k\beta-1)$ and k=$A/(\beta+A)$. It is clear

that not only capacitor mismatch but also the finite gain of amplifier have the direct influences on β-value. However, because the β-value are same for different conversion stage in cyclic ADC, the ADC output still keep linear in case of the β-encoding with effective stage gain of β_{eff}. According to Eq. (9), we see that not only the β-value but also the reference voltage of MDAC damages the linearity of ADC. Any reference voltage variation should cause the non-linearity at conversion stage. Careful design for reference circuits is necessary to guarantee the accuracy of the ADC, which cause the overhead of chip area and power penalty. Background calibration of proposed estimation technique can relieve the influence of reference voltage variation with required digital circuits.

3.2 Radix Value Estimation Algorithm

Although β-encoding provides an error correction technique for non-binary ADC, the β-encoding according to Eq. (2) is impractical without a certain radix value of β. Therefore, β-value estimation algorithm is needed to get the effective value of β_{eff}, and it enables to achieve the required linearity of ADC.

As shown in Fig. 6, we can get two conversion codes $D_1 = \{b_{01}, b_{02}, ..., b_{0n}\}$ (the MSB is 0) and $D_2 = \{b_{11}, b_{12}, ..., b_{1n}\}$ (the MSB is 1) corresponding to the same analog input in the range of $[v_1, v_2]$. When D_1 and D_2 are expressed by digital codes of b_{0n} and b_{1n}, we have

$$V_{in} = \sum_{n=1}^{\infty} \frac{1}{\beta^i} b_{0n} = \sum_{n=1}^{\infty} \frac{1}{\beta^i} b_{1n}. \tag{10}$$

Then we get

$$e(\beta) = \sum_{n=1}^{\infty} (b_{0n} - b_{1n}) \frac{1}{\beta^i} = 0. \tag{11}$$

The value of β can be calculated to satisfy the Eq. (11). It is clear that the value of β can be estimated simply without any adding circuits. The estimation is realized by the following steps:

i Input common-mode voltage to ADC. Normally, it only needs to shorten the differential inputs of ADC without analog input signal.
ii Starting AD conversion while MSB of ADC being fixed to 0, then gets the output code of b_{0n}.
iii Starting AD conversion while MSB of ADC being fixed to 1, then gets the output code of b_{1n}.
iv Calculate the value of β to satisfy the Eq. (11).

By this way, the effective value of β_{eff} can be estimated even the MDAC with capacitors mismatch and finite gain error. There is not any additional analog circuit is required to realize proposed algorithm. Only digital circuits are necessary to complete the calculation, which can be realized simply with nowadays CMOS technology.

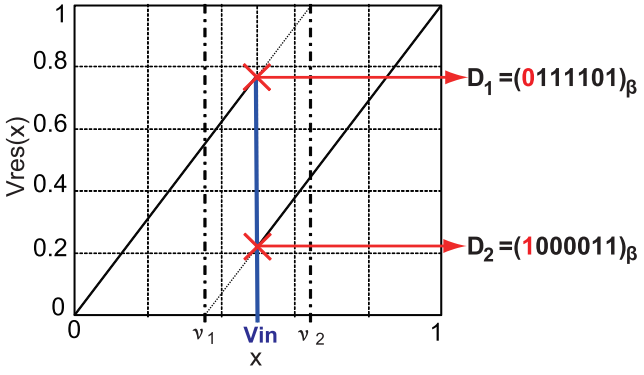


Fig. 6 The residue signal of radix-value estimation mode.

4. Simulation and Discussion

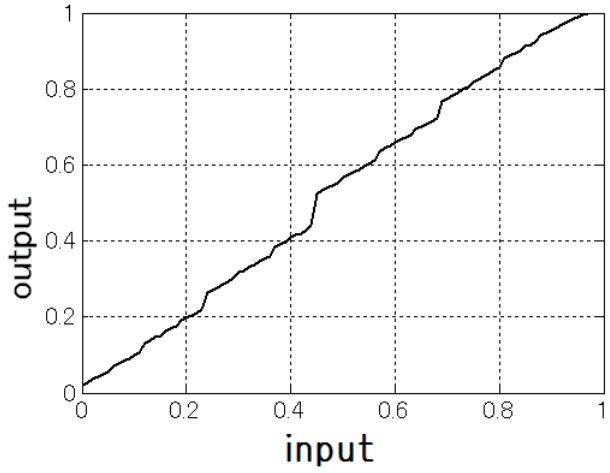
4.1 Validity of β-Expansion Method

MATLAB simulations have been conducted to confirm the robustness of the proposed ADC and effectiveness of estimation algorithm. In the behavioral model of the cyclic ADC as shown in Fig. 1, we assumed that β=1.8, the offset voltage of amplifier and comparator are 2.5% and 5% respectively. While the output of ADC is encoded in binary manner, as shown in Fig. 7(a), the linearity of ADC is greatly damaged. On the other hand, in case of the output code is encoded by Eq. (2), as shown in Fig. 7(b), the linearity of ADC is largely improved even with the non-ideal circuits.

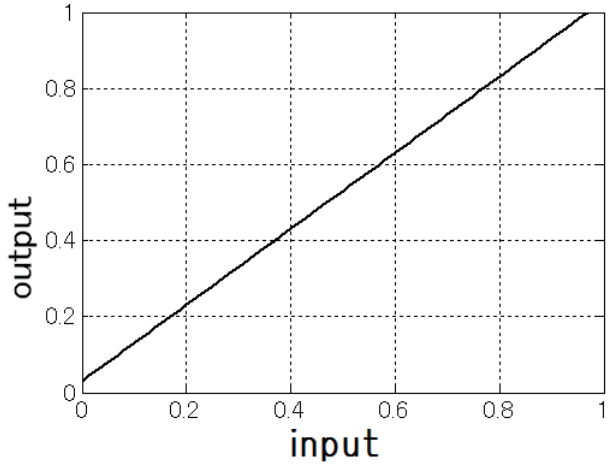
When we assume that β=1.9 and the DC gain of amplifier at the conversion stage is 40 dB, according to Eq. (9), the effective radix value should be β_{eff}=1.86457. In order to evaluate the rationality of above calculation, a MATLAB simulation for β-value estimation was run with above parameters. From the output code of the simulation results, the estimation error according to Eq. (11) is calculated, and the calculation results is shown in Fig. 8 while the value of β is swept with rate of 0.001/step. We see that the absolute value of e(β) is nearly to zero while β=1.8646. It is clear that the estimated value is nearly equal to the effective value of β calculated with Eq. (9). Therefore, we know that the right effective value of β can be estimated even with non-ideal circuits in non-binary ADC.

4.2 Proposed Architecture and Environmental Resistance

HSPICE simulations with TSMC90 nm CMOS process also been conducted to confirm the validity of conversion stage architecture to realized the β-expansion cyclic ADC. Gate-boosted NMOS switches are used at the input sampling parts of ADC to cancel the non-linearity of switch-ON-resistor, while all the others are CMOS switches. Non-overlapping clocks are provided to SWs in MDAC circuit to guarantee charge is not inadvertently lost. Latched comparator without any input offset-cancellation is used as the sub-ADC. Hence the proposed architecture tolerates poor gain amplifier and



(a) Binary encode



(b) β encode

Fig. 7 ADC transfer characteristics comparison.

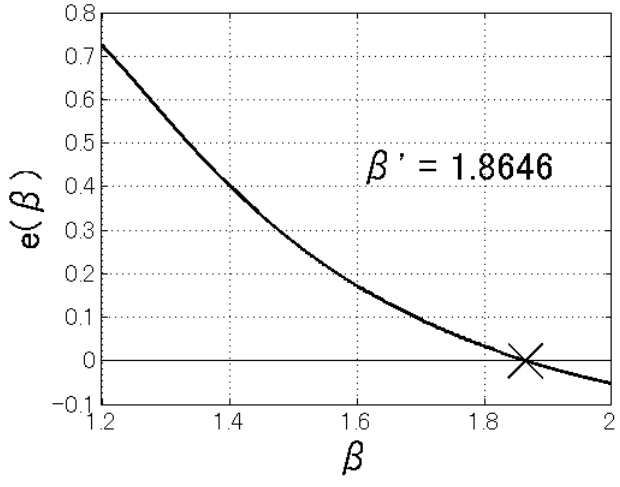


Fig. 8 β-value estimation error.

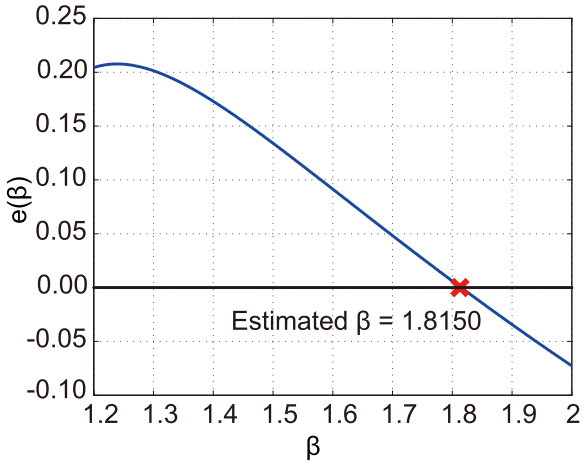


Fig. 9 Simulation results of β-value estimation.

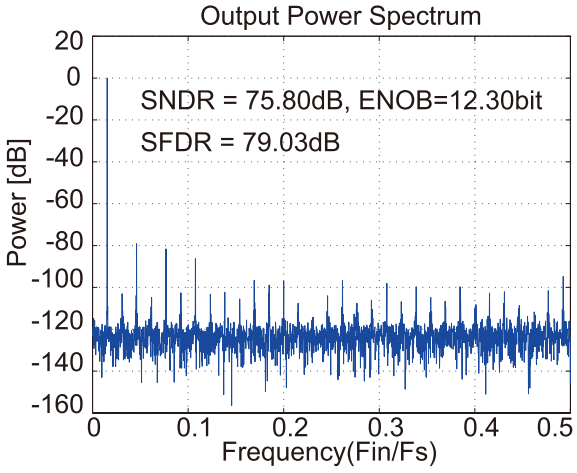


Fig. 10 Output power spectrum of cyclic ADC.

single stage folded-cascode amplifier is designed with the DC gain of as low as 50 dB at Vdd=1.2 V. The simulation results show the amplifier specification of PSRR=51.20 dB and CMRR= 65.79 dB.

Proposed cyclic ADC has β-value (radix-value) estimation mode and operation mode. In our simulation, reference level is $|V_{ref}|$=250 mV and common-mode voltage is V_{CM}=600 mV, then the reference voltage for ADC are $V_{ref1} = V_{CM} - V_{ref}$=350 mV and $V_{ref2} = V_{CM} + V_{ref}$=850 mV, sampling frequency is F_s = 1 MS/s and stage-gain of MDAC is β=1.8333. In the estimation mode simulation, the differential input of ADC was shortened. Figure 9 shows the e(β)-value results according to Eq. (11) while the value of β is swept, and the effective β-value is β_{eff} = 1.8150. In the operation mode simulation, the output codes of ADC are encoded as Eq. (2) corresponding to analog inputs. In our simulation, analog input signal is a sinusoidal wave of f_{in}=15.38 kHz with 1V_{pp}, β=β_{eff} by estimation mode result. Figure 10 shows the simulation result of output power spectrum of cyclic ADC with above estimated β-value. The peak SNDR achieved 75.80 dB even with a poor amplifier with

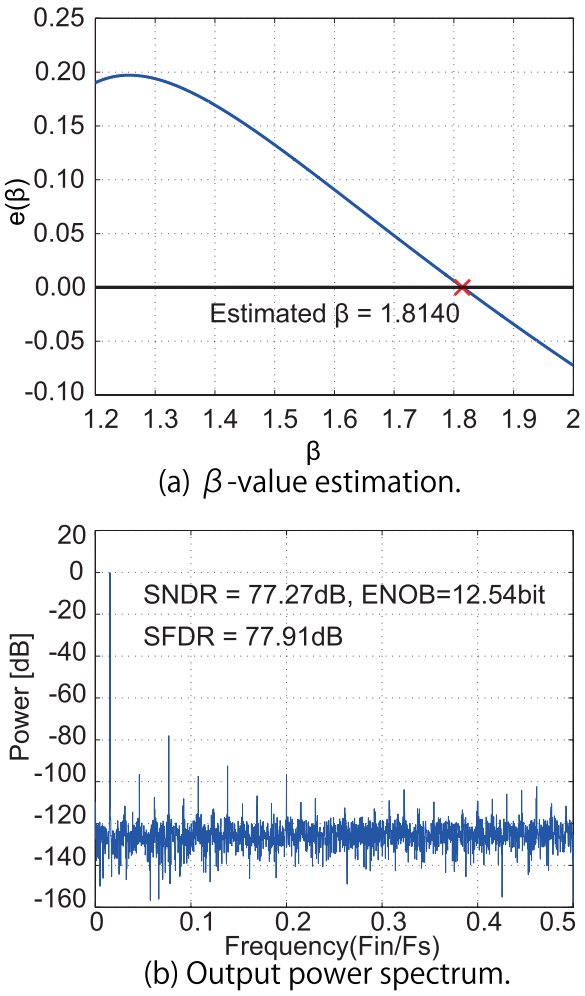


Fig. 11 ADC simulation results at low temperature (T = −20°C).

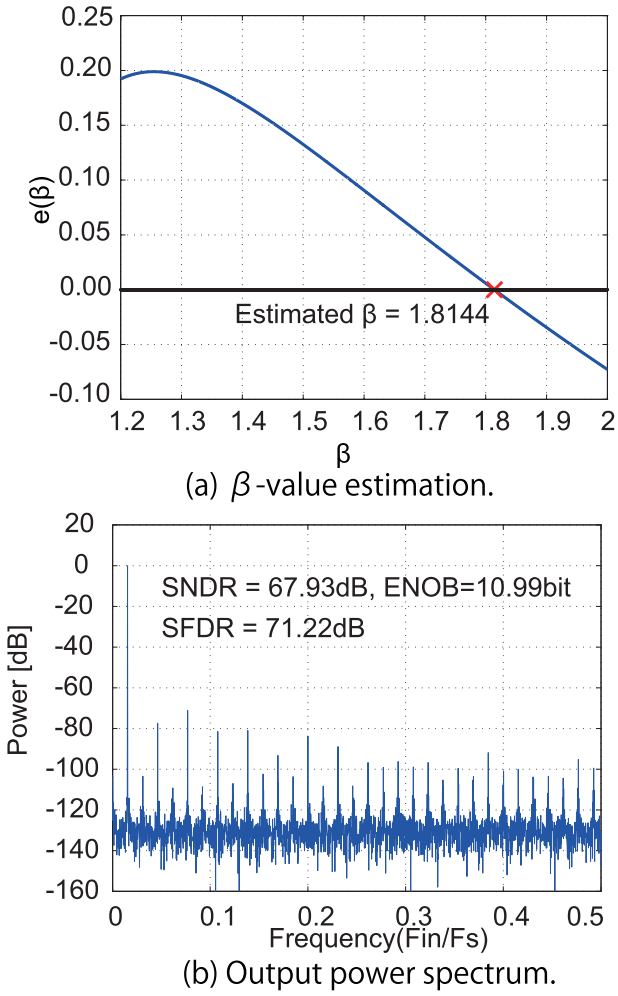


Fig. 12 ADC simulation results at high temperature (T=80°C).

DC gain is about 50 dB. Although the nonlinearity of analog SWs and amplifier caused harmonic distortions, which limited the performance of ADC, our simulation result shows that ENOB of ADC is more than 12 bits.

We also conducted simulation of verify the temperature characteristics to confirm the environmental resistance of proposed ADC. Figure 11 shows the simulation results of low temperature (T= −20°C). The effective β-value is β_{eff} = 1.8140, the peak SNDR is 77.27 dB. Similarly, Fig. 12 shows the results of high temperature (T=80°C). The effective β-value is β_{eff}=1.8144, the peak SNDR is 67.93 dB. In the case of high temperature, the accuracy of ADC is degrades. However, it has obtained to sufficient accuracy compared with the previous design method.

5. Conclusion

A non-binary cyclic ADC based on β-expansion with radix-value estimation algorithm is proposed. The redundancy of proposed ADC tolerates the conversion errors caused by coarse accuracy devices and circuit components. MATLAB and HSPICE simulation results demonstrate the validity of proposed ADC architecture and the effectiveness of proposed radix-value estimation algorithms. These results show the feasibility of robust ADC with deep submicron CMOS technologies beyond 90 nm.

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Rie Suzuki received the B.S. degree in Information network engineering from Musashi Institute of Technology in 2011, M.S. degree in information engineering from Tokyo City University in 2013, respectively. Her research interests lie in CMOS circuits design of AD converters.

Tsubasa Maruyama received the B.S. degree in electronic communication engineering from Musashi Institute of Technology in 2010. M.S. degree in information engineering from Tokyo City University in 2012, respectively. His research interests lie in CMOS circuits design of AD converters.

Hao San received the B.S. degree in Automation Engineering from Liaoning Institute of Technology, China in 1993, the M.S. and Dr. Eng. degrees in Electronic Engineering from Gunma University, Japan, in 2000 and 2004, respectively. From 2000 to 2001, he worked with Kawasaki Microelectronics Inc.. He joined Gunma University as an Assistant Professor in the Department of Electronic Engineering in 2004. In 2009 he joined Tokyo City University as an Associate Professor in the Department of Information Network Engineering. His research interests include analog and mixed-signal integrated circuits. Dr. San is an Associate Editor of IEICE Transactions on Electronics from 2010. He also serveed as a Treasurer of IEEE Circuits and Systems Society Japan Chapter from 2011 to 2012. He is a member of the IEEE and IEEJ.

Kazuyuki Aihara received the B.E. degree of electrical engineering in 1977 and the Ph.D. degree of electronic engineering 1982 from the University of Tokyo, Japan. Currently, he is Professor of Institute of Industrial Science, the University of Tokyo, Professor of Graduate School of Information Science and Technology, the University of Tokyo, and Director of Collaborative Research Center for Innovative Mathematical Modelling, the University of Tokyo. His research interests include mathematical modeling of complex systems, parallel distributed processing with spatio-temporal chaos, and time series analysis of complex data.

Masao Hotta received the Ph.D. degree in electronics from Hokkaido University, Sapporo, Japan, in 1976. In 1976 he was with the Central Research Laboratory, Hitachi Ltd., Tokyo, Japan. He engaged in research and development of high-precision D/A converters, ultrahigh- speed D/A converters and highspeed A/D converters. From 1996 to 2003, he was a Manager of Advanced Device Development Department and also a Senior Chief Engineer & Senior Manager of Advanced Analog Technology Center, Semiconductor & Integrated Circuits Division of Hitachi Ltd. He has worked on the development of mixedsignal LSIs, He conducted development on RF power amplifier modules, RF transceiver LSIs, mixed-signal LSIs and advanced analog cores for SoC. Since 2005, he has been a Professor at Tokyo City University, Tokyo, Japan, working on high performance ADCs, mixed-signal LSI design and wireless systems. Dr. Hotta has served as a chair of IEEE Circuits and Systems Society Japan Chapter, technical program committee members of CICC, BCTM and ASIC/SOC Conference and a chair of Technical Committee on Circuits and Systems, IEICE. He is a fellow of IEEE.