PAPER Special Section on Analog Circuit Techniques and Related Topics

Non-binary Pipeline Analog-to-Digital Converter Based on β-Expansion

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SUMMARY This paper proposes a pipeline analog-to-digital converter (ADC) with non-binary encoding technique based on β-expansion. By using multiply-by-β switched-capacitor (SC) multiplying digital-to-analog converter (MDAC) circuit, our proposed ADC is composed by radix-β ($1 < \beta < 2$) 1 bit pipeline stages instead of using the conventional radix-2 1.5 bit/1 bit pipeline stages to realize non-binary analog-to-digital conversion. Also with proposed β-value estimation algorithm, there is not any digital calibration technique is required in proposed pipeline ADC. The redundancy of non-binary ADC tolerates not only the non-ideality of comparator, but also the mismatch of capacitances and the gain error of operational amplifier (op-amp) in MDAC. As a result, the power hungry high gain and wide bandwidth op-amps are not necessary for high resolution ADC, so that the reliability-enhanced pipeline ADC with simple amplifiers can operate faster and with lower power. We analyse the β-expansion of AD conversion and modify the β-encoding technique for pipeline ADC. In our knowledge, this is the first proposal architecture for non-binary pipeline ADC. The reliability of the proposed ADC architecture and β-encoding technique are verified by MATLAB simulations.

key words: *non-binary AD conversion, β-expansion, pipeline ADC, switched-capacitor circuits, multiply-by-β MDAC*

1. Introduction

Pipeline analog-to-digital converter (ADC) is a popular architecture in many mixed-signal processing applications of multimedia consumer electronics, portable communications and image processing systems. As an interface between the analog world and the digital domain, ADCs are required with the performances of higher resolution, high speed and low power consumption with small chip area. CMOS process continues to shrink into nanometer scale according to ITRS load map [1]. Digital circuits benefit from high speed, high density and low power. However, low supply voltage and the device characteristics degradation such as threshold voltage mismatch of transistor pair and reduction of drain output resistance r_{ds} damage the accuracy of analog circuits. Especially, it limits the performance of amplifier which is one of the key components of pipeline ADC.

In conventional 1 bit/stage switched-capacitor (SC) binary pipeline ADC, the linearity of ADC is sensitive to not only the offset of amplifier and/or comparator caused by mismatch of transistors, but also the interstage gain errors which caused by capacitor mismatch and the finite DC gain of amplifier used in multiplying digital-to-analog converter (MDAC). Pipeline ADCs with 1.5 bit/stage architecture have been proposed to tolerate the non-ideality in each pipeline stage. With the redundancy of 1.5 bit architecture in each sub-conversion stage [2], [3], the ADC can be implemented insensitive to the offset of amplifier and comparator. The error correction using the redundant bit at each pipelined stage becomes the most popular technique for pipeline ADCs. However, the linearity of ADC is still seriously damaged by the capacitor mismatch and poor DC gain of amplifier, especially in nano-meter CMOS process. Therefore, high accuracy matched capacitors and power hungry high DC gain amplifier are necessary to satisfy the required ADC linearity. Although digital calibration techniques have been proposed to relax the required performance of the analog elements in pipeline ADC [4], the algorithms and their realization circuits are still complex, and calibration time is too long to be used effectively [5].

A non-binary analog-to-digital conversion technique based on β-expansion [6]–[10] has been proposed to overcome the offset error in sub-ADC. The error correction technique called β-encoding can improve the linearity of ADC with redundant digital output code. However, there are two limitations on providing the β-encoding for pipeline ADC, (1) the values of β realized by the ratio of capacitors are uncertain because of the inaccuracy of capacitor matching; and (2) the values of β are different at each pipeline stage. A bit stream embedding method has been proposed to realize the β-encoding with uncertain value of β [11], however, two high accuracy analog input signals are necessary for this method, which is impractical for a pipeline ADC.

In order to apply the reduandancy of non-binary analog-to-digital conversion to tolerates the non-ideality of analog circuits, we modified the β-encoding technique to be suitable for pipeline ADCs [12]. We also propose the non-binary 1 bit/stage pipeline ADC implementation by switched-capacitor circuits. The robustness of the proposed non-binary pipeline ADC tolerates not only the offset of comparator but also the mismatch of capacitors in MDAC at each pipeline stage.

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2. Pipeline ADC Based on β-Expansion

2.1 β-Encoding of Pipeline ADC

Figure 1 shows the block diagram of an N-stage pipeline ADC with 1 bit/stage architecture. Each conversion stage contains a 1 bit sub-ADC, a 1 bit digital-to-analog converter (DAC), an analog subtractor, and a gain amplifier. Each stage resolves one bit and sends the residual signal to next pipeline stage. The 1 bit conversion stage is similiar to the conventional structure, however, a multiply-by-β ($1<\beta<2$) amplifier is used instead of using a gain-of-2 amplifier, and the output of DAC is scaled by $\beta-1$. While the output code of sub-ADC in the Mth-stage is b_M (b_M= 0 or 1), corresponding the output voltage of 1 bit DAC is 0 or V_{FS} (the full scale voltage of the analog input signal), then the residue of the 1st, 2nd and 3rd stages can be expressed as

$$V_{res1} = \beta V_{in} - b_1(\beta-1)V_{FS} \quad (1)$$

$$\begin{aligned} V_{res2} &= \beta V_{res1} - b_2(\beta-1)V_{FS} \\ &= \beta[\beta V_{in} - b_1(\beta-1)V_{FS}] - b_2(\beta-1)V_{FS} \end{aligned} \quad (2)$$

$$\begin{aligned} V_{res3} &= \beta V_{res2} - b_3(\beta-1)V_{FS} \\ &= \beta\{\beta[\beta V_{in} - b_1(\beta-1)V_{FS}] \\ &\quad - b_2(\beta-1)V_{FS}\} - b_3(\beta-1)V_{FS}. \end{aligned} \quad (3)$$

Equation (3) also can be written as

$$V_{res3} = \beta^3 V_{in} - (\beta-1)(\beta^2 b_1 + \beta^1 b_2 + \beta^0 b_3)V_{FS}, \quad (4)$$

while dividing by $V_{FS}\beta^3$, Eq. (4) can be expressed as

$$\frac{V_{in}}{V_{FS}} = (\beta-1)\left(\frac{b_1}{\beta} + \frac{b_2}{\beta^2} + \frac{b_3}{\beta^3}\right) - \frac{1}{\beta^3}\frac{V_{res3}}{V_{FS}}. \quad (5)$$

Thus, for a pipeline ADC with N stages, we have

$$\frac{V_{in}}{V_{FS}} = (\beta-1)\sum_{n=1}^{N}\frac{1}{\beta^n}b_n - \frac{1}{\beta^N}\frac{V_{resN}}{V_{FS}}. \quad (6)$$

Equation (6) means that the ratio of the analog input V_{in} to V_{FS} can be expressed as a digital code series of $[b_N, b_{N-1}, ..., b_2, b_1]$ (the outout codes of N-stage sub-ADCs)

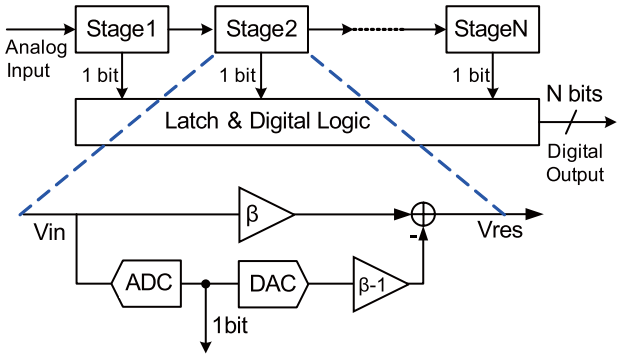

Fig. 1 Block diagram of 1 bit/stage pipeline ADC.

and quantization error. Then, we call the following mapping equantion as β-encoding of analog signal.

$$\frac{V_{in}}{V_{FS}} = (\beta-1)\sum_{n=1}^{N}\frac{1}{\beta^n}b_n \quad (7)$$

According to Eq. (7), in the case of $\beta = 2$, the pipeline ADC operation is in a binary manner. The linearity of the ADC is very sensitive to the offset of comparator, inaccurate interstage gain caused by mismatch of capacitors and finite DC gain of amplifier. Alternatively, in the case of $1<\beta<2$, the ADC operation is in a non-binary manner. Note the 2nd term at right side of Eq. (6), since the residue of the last pipeline stage is the quantization error of the ADC, then we know that $1/2^N < 1/\beta^N$. It is obvious that the resolution of each pipeline stage in non-binary ADC with radix $\beta<2$ is less than that of binary ADC. Therefore, while $1<\beta<2$, more pipeline conversion stages are necessary for required resolution of binary ADC. Normally, in order to realize a binary ADC with N-bit resolution, the required stage number M of non-binary ADC must satisfy the formula of $1/\beta^M < 1/2^N$. With the redundancy of non-binary ADC, the required circuit performance can be largely relaxed, and the robustness of non-binary ADC tolerates the inaccurate interstage gain at each pipeline stage.

2.2 Modified β-Encoding for Pipeline ADC

In the fomulation of Eqs. (1)–(7), all values of β are the same at each pipeline stage in the ideal case. However, it is impractical because the random mismatch of capacitors cause the variation of β-value at different pipeline stages. To garantee the linearity of pipeline ADC with different β-value at different stages, we modify the Eq. (1) to Eq. (7) with different β as $\beta_1, \beta_2, \beta_3$,..., then we have,

$$\begin{aligned} V_{res1} &= \beta_1 V_{in} - b_1(\beta_1-1)V_{FS}, \\ V_{res2} &= \beta_2[\beta_1 V_{in} - b_1(\beta_1-1)V_{FS}] - b_2(\beta_2-1)V_{FS}, \\ V_{res3} &= \beta_3\{\beta_2[\beta_1 V_{in} - b_1(\beta_1-1)V_{FS}] \\ &\quad - b_2(\beta_2-1)V_{FS}\} - b_3(\beta_3-1)V_{FS}. \end{aligned} \quad (8)$$

Equation (8) also can be written as

$$\begin{aligned} V_{res3} &= \beta_3\beta_2\beta_1 V_{in} - \beta_3\beta_2(\beta_1-1)b_1 V_{FS} \\ &\quad -\beta_3(\beta_2-1)b_2 V_{FS} - (\beta_3-1)b_3 V_{FS}, \end{aligned} \quad (9)$$

while dividing by $V_{FS}\beta_3\beta_2\beta_1$, Eq. (9) can be expressed as

$$\frac{V_{in}}{V_{FS}} = \frac{\beta_1-1}{\beta_1}b_1 + \frac{\beta_2-1}{\beta_2\beta_1}b_2 + \frac{\beta_3-1}{\beta_3\beta_2\beta_1}b_3 - \frac{1}{\beta_3\beta_2\beta_1}\frac{V_{res3}}{V_{FS}}. \quad (10)$$

Thus, for a pipeline ADC with N stages, we have

$$\frac{V_{in}}{V_{FS}} = \sum_{n=1}^{N}(\beta_n-1)\frac{1}{\Pi_{m=1}^{n}\beta_m}b_n - \frac{1}{\Pi_{m=1}^{N}\beta_m}\frac{V_{resN}}{V_{FS}}. \quad (11)$$

Also, the mapping equantion of β-encoding is modified as

$$\frac{V_{in}}{V_{FS}} = \sum_{n=1}^{N}(\beta_n - 1)\frac{1}{\Pi_{m=1}^{n}\beta_m}b_n \tag{12}$$

As a result, we know that for a non-binary pipeline ADC, it is necessary to encode the output code of each sub-ADC as the Eq. (12) to achieve the linearity of the whole ADC. It is obvious that when the values of β are the same at each pipeline stage, Eq. (12) is the same as Eq. (7); also when β are the same at all stages as β=2, then Eq. (12) can be simplified to an ideal case of binary encoding as follows:

$$\frac{V_{in}}{V_{ref}} = \sum_{n=1}^{N}\frac{1}{2^n}b_n \tag{13}$$

Figure 2 shows simulated input-output transfer characteristic of non-binary pipeline ADC with MATLAB. An 8-stage pipeline ADC is simulated, the interstage gain of ADC determined by the value of β is 1.86 with 0.5% random gain error at each pipeline stage. While the output code of 6-MSBs is calculated using Eq. (13) in the binary manner, as shown in Fig. 2(a), the transfer curve becomes non-linear because of the gain error at each stage. On the other hand, while the 8-bit output code is calculated using Eq. (12) with different real β-value of each stages, the transfer curve becomes linear by the error correction of β-encoding as shown in Fig. 2(b). It should be noted that for the simulation results comparision, the 8-bit output code of non-binary ADC is normalized to the output code of 6-bit binary ADC.

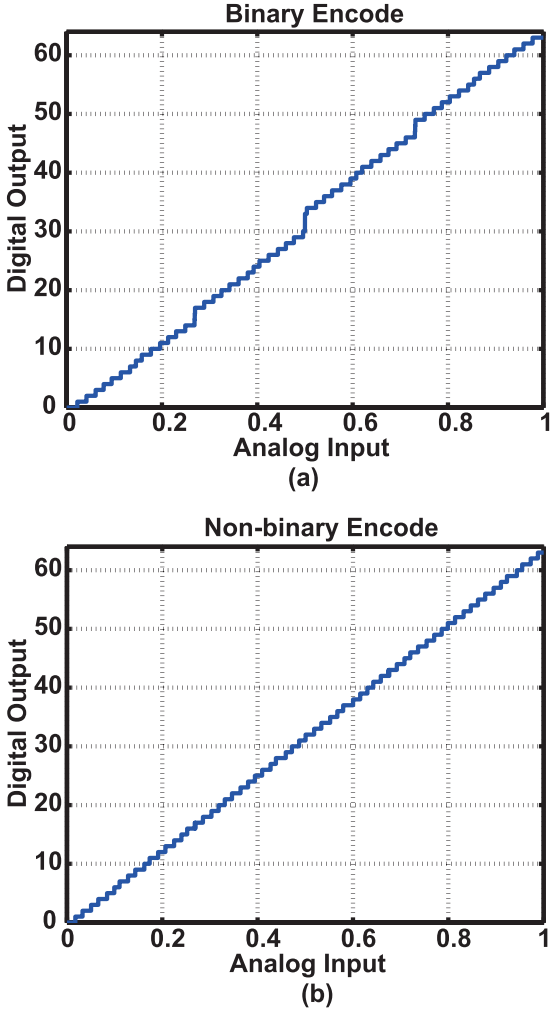

Fig. 2 ADC transfer characteristic. (a) Binary encode. (b) Non-binary encode.

3. Proposed Non-binary Pipeline ADC Architecture

Although β-encoding provides an error correction technique to realize a robust non-binary ADC, some technical problems limit the possibility for their implementation. The problems are (a) multiply-by-β circuit configuration should be addressed to satisfy the transfer function expressed as Eq. (1); and (b) β-encoding is impractical without finding correct value of β. Regarding to above problems, we proposed a simple multiply-by-β pipeline stage to realize the transfer function of Eq. (1) to get the output digital code for β expansion. We also proposed a β-value estimation algorithm for above pipeline stage to provide the exact radix value for β-encoding.

3.1 Multiply-by-β Pipeline Stage

An multiply-by-β pipeline structure has been proposed in [4] to realize the pipeline stage of radix $\beta < 2$ by adding an extra capacitor and switches to the conventional multiply-by-2 MDAC circuit. Not only the circuit is complex, but also the transfer function at each pipeline stage is different from Eq. (1). Figure 3 shows the SC implementation of each stage for proposed non-binary pipeline ADC. Although a single-ended configuration is shown for simplicity, the actual implementation is fully differential. The operation of simplified multiply-by-β amplifier is illustrated in Fig. 4. During the sampling phase, the analog input V_{in} is sampled by the capacitors C_s and C_f. During the amplifying phase, C_f is connected to the output of the amplifier V_{res} and C_s is connected to the reference voltage of $+V_{ref}$ or $-V_{ref}$, depending on the output stage of sub-ADC, d_n (d_n =1 or −1). According to the charge conservation law, and assuming that the DC gain of amplifier is infinite, then the residue of pipeline stage is expressed as

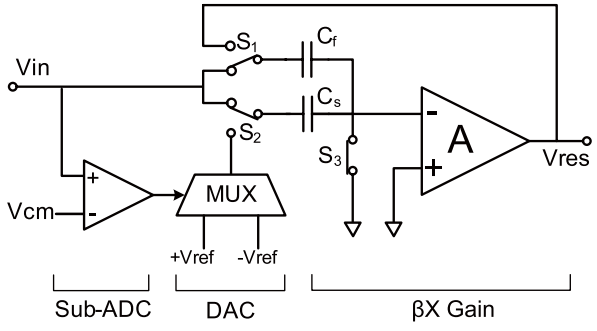

Fig. 3 Switched-capacitor implementation of pipeline stage.

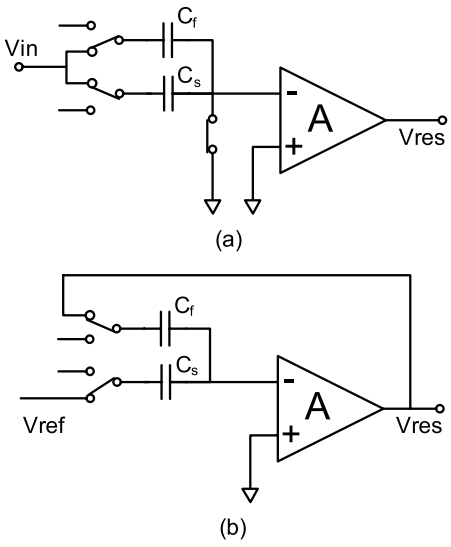

Fig. 4 Switched-capacitor multiply-by-β amplifier. (a) Sampling phase. (b) Amplifying phase.

$$V_{res} = \frac{C_s + C_f}{C_f} V_{in} - d_n \frac{C_s}{C_f} V_{ref}. \quad (14)$$

We see that the SC circuit is the same as the conventional multiply-by-2 MDAC in the case of C_s=C_f, however, while we make C_s=$(\beta - 1)C_f$, the transfer function expressed as

$$V_{res} = \beta V_{in} - d_n(\beta - 1)V_{ref}. \quad (15)$$

Equation (15) shows that multiply-by-β amplification is realized simply only by changing the ratio of capacitors around MDAC. Although the same MDAC configuration have been used in [13] to get attenuation of analog signal to avoid the missing codes, the pipeline ADC with interstage gain less than 2 is still need a complexity analog calibration sequence. As explained later, in our proposed non-binary ADC architecture, because the uncertain interstage gain (the ratio of capacitors) of pipelined ADC can be estimated, neither accurate matching of capacitors, nor calibration technique needed in our proposed non-binary ADC architecture. We just use this simple multiply-by-β structure to get the output code for β-encoding, and get the ADC output in non-binary mannar with different radix values of β in the different pipeline stage.

3.2 β-Value Estimation Algorithm

In the 1 bit/stage pipeline ADC with interstage gain is 2, any non-ideality such as comparator offset and capacitor mismatch will damage the linearity of ADC [13]. The dotted line in Fig. 5(a) shows the transfer characteristic of first pipeline stage with comparator offset. Over-ranged residue will cause the miss code at the output of ADC. On the other hand, while the interstage gain is less than 2, as shown in Fig. 5(b), the residue is still in allowed-range of the next pipeline stage even the comparator with offset is used. Thus, the ADC output can be kept linear by β-encoding based on

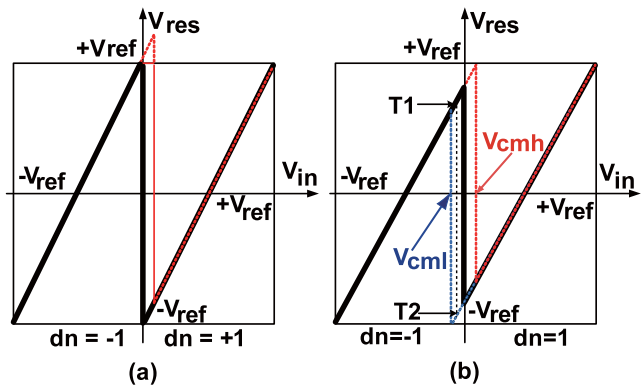

Fig. 5 Transfer characteristic of the switched-capacitor pipeline stage. (a) radix = 2. (b) radix = $\beta < 2$.

Eq. (12). However, it is clear that the β-encoding according to Eq. (12) is impractical without a certain value of β. The capacitor mismatch will cause the random variation of β-value even if we have decided it by the ratio of capacitors. Therefore, we proposed a β-value estimation algorithm to get the value of β for encoding to satisfy the required linearity of ADC [14].

The idea is very simple which comes from the redundancy of non-binary ADC. Note the transfer curve of the first pipeline stage with interstage gain β shown in Fig. 5(b), the allowable comparator offset is in the range of (V_{cml}, V_{cmh}). In other word, while the anglog input signal is in the range of (V_{cml}, V_{cmh}), it can be expressed with two different digital codes. For example, the points $T1$ and $T2$ in Fig. 5(b) correspond to the same analog input. While the multiply-by-β pipeline stage operates as a cyclic ADC, we can get two conversion code, $D1$ is the digital code of point $T1$, and $D2$ is the digital code of point $T2$, corresponding to the same analog input. It is clear that the MSB of $D1$ is '0', and the MSB of $D2$ is '1'. Different from the binary ADC, in the non-binary ADC with redundant bit, the same analog input can be expressed by two different digital codes. Therefore, from equation $D1 = D2$, the value of β can be calculated according to Eq. (7). Moreover, in the estimation mode of ADC, there is not any extra analog input signal used because we short the input nodes of differential pair to get the same analog input for ADC. A pair of digital output codes can be obtained by we started the AD conversion after set the MSB of DAC as 0 or 1 despite the offset of comparator.

In a cyclic ADC, the same conversion stage is used step by step, the value of β are the same at different conversion stages, so that above estimation algorithm can be used directly to get the effective β-value of ADC However, in a pipeline ADC, the different stages are used to resolve different analog signals, and the value of β is different at each stage. Normally, the operation of proposed pipeline ADC can be consider as two mode, estimation mode and conversion mode. In estimation mode, all convertion stages are set as cyclic ADCs, and above algorithm can be applied to them to get the β-value of each stage; On the other hand,

in conversion mode, all conversion stages are cascaded as a pipeline ADC, the output codes of ADC are encoded according to Eq. (12) with estimated effective β-values for all pipelined stages. Although applying above estimation algorithm to all pipeline stages is the ideal way to get effective β-values of all stages, it is inefficient to estimate them for circuit implementation. Since the weight of MSBs is larger than that of LSBs, we just need to estimate the β-value of MSB-stages (Ex. $\beta_1, \beta_2, \beta_3$), and use the average value of MSBs (Ex. $\beta_{ave} = (\beta_1 + \beta_2 + \beta_3)/3$) as the β-value for other LSB-stages. Furthermore, the necessary estimation stage number of MSB-stages shouled be decided by system level simulation to satisfy the required resolution of the ADC.

4. Simulation and Discussion

In order to confirm the validity of the proposed architecture and β-value estimation algorithm, we conducted the MATLAB simulation with the behavioral model of the pipeline ADC with 13 pipeline stages. The interstage gain of ADC is 1.86 with 0.5% random error of 3σ standard deviation in Gaussian distribution at each stage. The 13 bits non-binary output codes are used to realize a 10-bit binary ADC.

Firstly, in order to make clear the ADC resolution dependence on accuracy of β-value estimation, we make the comparison of SNDR with the accuracy of β-value. Figure 6 shows the simulation results of SNDR of ADC vs. estimation error of β-value in case of ADC with required resolution of 10-bits. We see that in order to achieve the ADC resolution not less than 55.9 dB(9-bits), the β-value estimation error must be less than 0.28%.

Secondly, we did Monte Carlo simulation to comfirm the necessary estimation stage number to achieve the required ADC resolution of 10-bits. In our simulation, we assumed that ideally estimated β-values $(\beta_1, \beta_2, \cdots, \beta_n)$ are applied to n-MSB-stages; and the average value of n-MSBs ($\beta_{ave}=\sum_{m=1}^{n}\beta_m/n$) are applied to other (n-1)-LSB-stages ($\beta_{ave}=\beta_{n+1}=\beta_{n+2}=\cdots=\beta_{10}$). The histogram of 10,000 samples of simulation result of ENOB (Effective Number Of Bits) for the cases of n=2, 3, 4 and 5 are shown in Fig. 7. While ideally estimated β-values were applied to 2-MSB-stages, the most frequency case is that the ADCs' ENOB are less than 9.5-bits. While ideally estimated β-values were applied to 3-MSB-stages, the most frequency case of ENOB is more than 9.9-bits, however, sometimes the ENOB of ADC are less than 9.8-bis. On the other hand, while ideally estimated β-values were applied to 4 or 5 MSB-stages, the histogram results show that the ENOB of ADC are higher than 9.9-bits more than 95% frequency. From above simulation

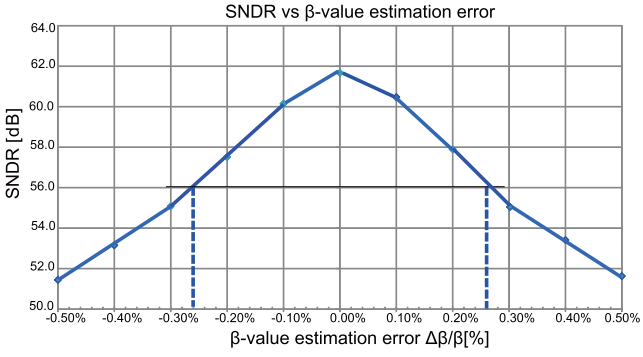

Fig. 6 SNDR of ADC vs. β-value estimation error.

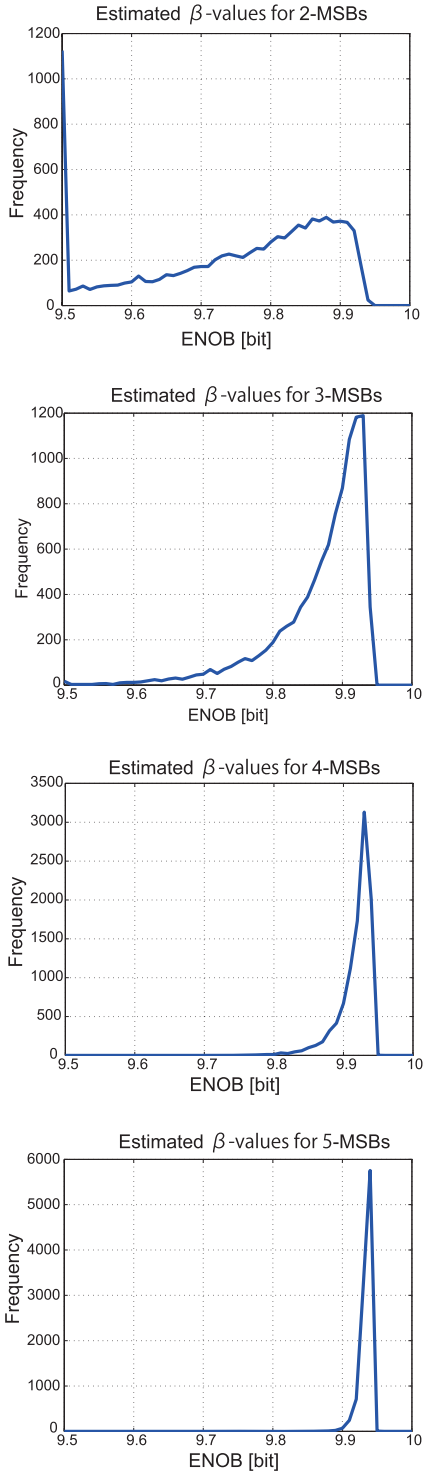

Fig. 7 Histogram of ADC ENOB by Monte Carlo simulation in the difference cases of ideally estimated β-values are applied.

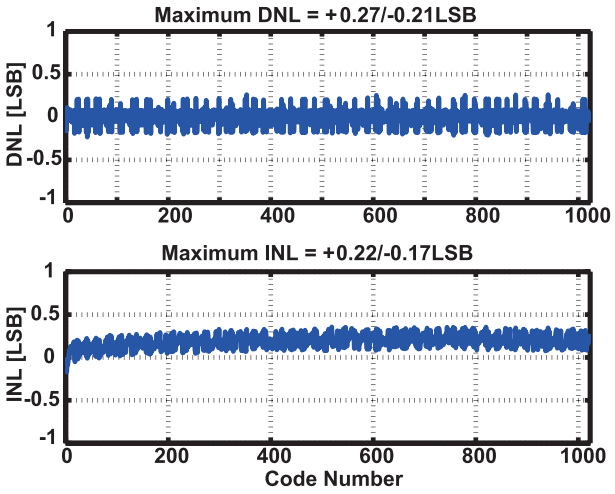

Fig. 8 DNL, INL of non-binary ADC with ideal interstage gain pipeline stages.

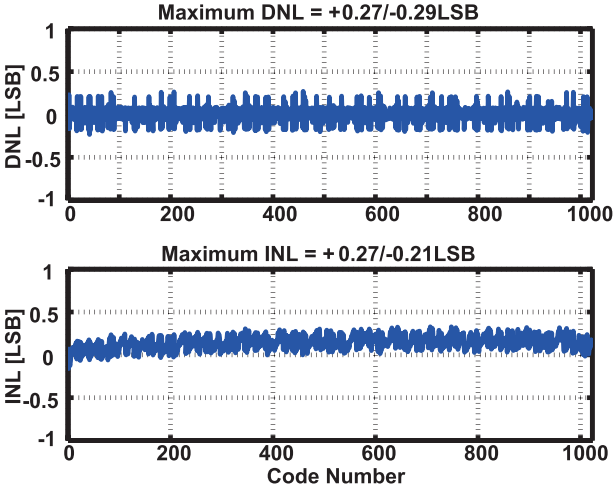

Fig. 9 DNL, INL of non-binary ADC with non-ideal interstage gain pipeline stages.

results and disscusion, we see that in our behavioral model of pipeline ADC, we have to estimate 4-MSB-stages in a 13-stages pipeline ADC to achieve the 10-bits resolution.

We also calculate the DNL and INL of simulated ADC to confirm the effectiveness of the proposed architecture and β-value estimation algorithm. While the values of β at all stages are ideally estimated, the DNL and INL results shown in Fig. 8 are less then ± 0.5LSB. On the other hand, we assume that only 4-MSBs interstage gain are estimated, for the other 9 stages, the average value of 4-MSBs are used as the value of β. The simulation results of DNL and INL are shown in Fig. 9. From these simulation results, we see that the DNL and INL are less than ± 0.5LSB, even with 9 non-ideal interstage gain in the pipeline ADC. The redundancy of non-binary ADC tolerates non-ideal characteristic to satisfy the required resolution.

5. Conclusion

We proposed multiply-by-β MDAC architecture to realize a non-binary pipeline ADC based on β-expansion. To realize the error correction for non-binary the pipeline ADC, we modified the β-encoding technique to keep the linearities of ADC with non-ideal interstage gains at different pipeline stage. We also proposed β-value estimation algorithm to realize the β-encoding even with uncertain capacitor mismatch in the proposed circuits. The MATLAB simulation results with behavioral model verified the effectiveness of the proposed circuits and algorithm. In our proposed pipeline ADC, only simple 1 bit/stage multiply-by-β architecture is used. Since the interstage gain is less than 2, the ADC tolerates the comparator offset even with 1 bit/stage architecture. Furthermore, because the interstage gain value of β can be estimated from output codes of ADC, the matching accuracy of capacitors can be relaxed. The robustness of of proposed ADC is suitable for the mixed-signal processing with deep sub-micro CMOS process.

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