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PAPER Special Section on Analog Circuit Techniques and Related Topics

A 6th-Order Quadrature Bandpass Delta Sigma AD Modulator Using Dynamic Amplifier and Noise Coupling SAR Quantizer

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SUMMARY This paper presents a 6th-order quadrature bandpass delta sigma AD modulator (QBPDSM) with 2nd-order image rejection using dynamic amplifier and noise coupling (NC) SAR quantizer embedded by passive adder for the application of wireless communication system. A novel complex integrator using dynamic amplifier is proposed to improve the energy efficiency of the QBPDSM. The NC SAR quantizer can realize an additional 2nd-order noise shaping and 2nd-order image rejection by the digital domain noise coupling technique. As a result, the 6th-order QBPDSM with 2nd-order image rejection is realized by two complex integrators using dynamic amplifier and the NC SAR quantizer. The SPICE simulation results demonstrate the feasibility of the proposed QBPDSM in 90 nm CMOS technology. Simulated SNDR of 76.30 dB is realized while a sinusoid −3.25 dBFS input is sampled at 33.3 MS/s and the bandwidth of 2.083 MHz (OSR=8) is achieved. The total power consumption in the modulator is 6.74 mW while the supply voltage is 1.2 V.

key words: *quadrature bandpass delta sigma modulator, image rejection, SAR quantizer, noise coupling, ring amplifier, complex integrator*

1. Introduction

In wireless communication systems, the digital signal processing with complex signals is widely used in the receiver circuit. High speed, high resolution, low power consumption Analog-to-Digital Converter (ADC) is necessary in both I-channel and Q-channel complex signal paths, respectively. Due to the performance of the baseband receiver (low-frequency receiver) circuit using Nyquist-rate ADC is easily affected by the DC-offset and the flicker noise (1/f noise), the quadrature bandpass delta sigma AD modulator (QBPDSM) is proposed [1] for reducing the influence of the DC-offset and the flicker noise. QBPDSM can be used in the mixed-signal system-on-chip (SoC) in the fields of both the digital radio [2] and the gyro sensor. Several techniques have been proposed to improve the performance and the energy efficiency of QBPDSM. Image rejection technique is proposed [1] to reduce the influence of the mismatch of I and Q paths. Multi-bit internal quantizer can relax the slew-rate requirement on the amplifier to reduce the power consumption of the modulator [3]. Feed-forward structure is used to reduce the output swing of the integrator, which can relax the linearity requirements on the amplifier in the integrator, and can reduce the power consumption of the delta sigma AD modulator [4]. For realizing

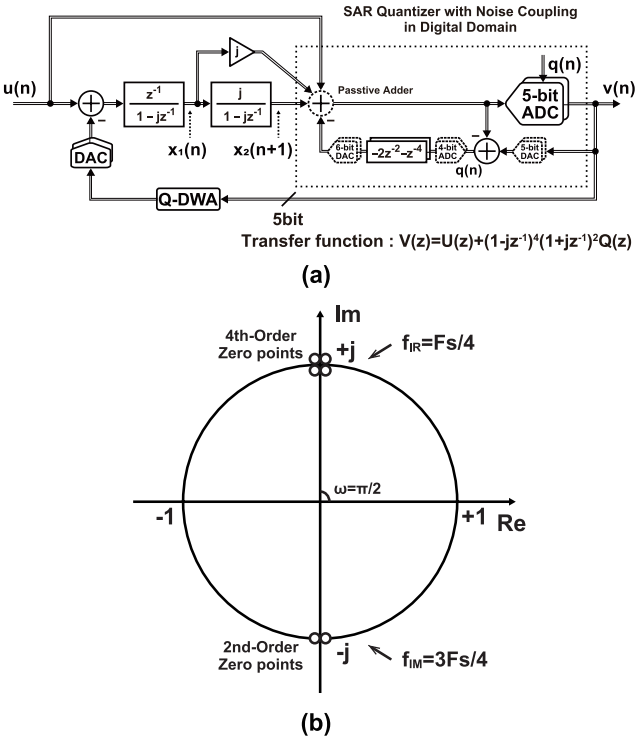

Fig. 1 Architecture of proposed 6th-Order complex bandpass delta sigma modulator, (a) Signal flow diagram. (b) Zero points of noise transfer function.

the integration of the complex signal, the traditional complex integrator circuit is proposed in the previous work [1]. The amplifiers used to achieve the traditional complex integrator circuit perform twice charge transfer actions (two operation phases are required) for once integration operation of complex signal, which accompany the high power consumption and the low energy efficiency. In this work, a novel implementation of complex integrator circuit is proposed for improving the energy efficiency and reducing the circuit area of QBPDSM. The dynamic amplifier instead of the operational transconductance amplifier (OTA) is used to implement the complex integrator circuit for maximizing the power efficiency of the amplifier. The proposed complex integrator only requires once charge transfer action for once complex integration operation, which can reduce the power consumption of QBPDSM. Furthermore, the load capacitance of proposed complex integrator circuit is half compare with the conventional complex integrator, which can reduce the circuit area of QBPDSM. Moreover, in order to

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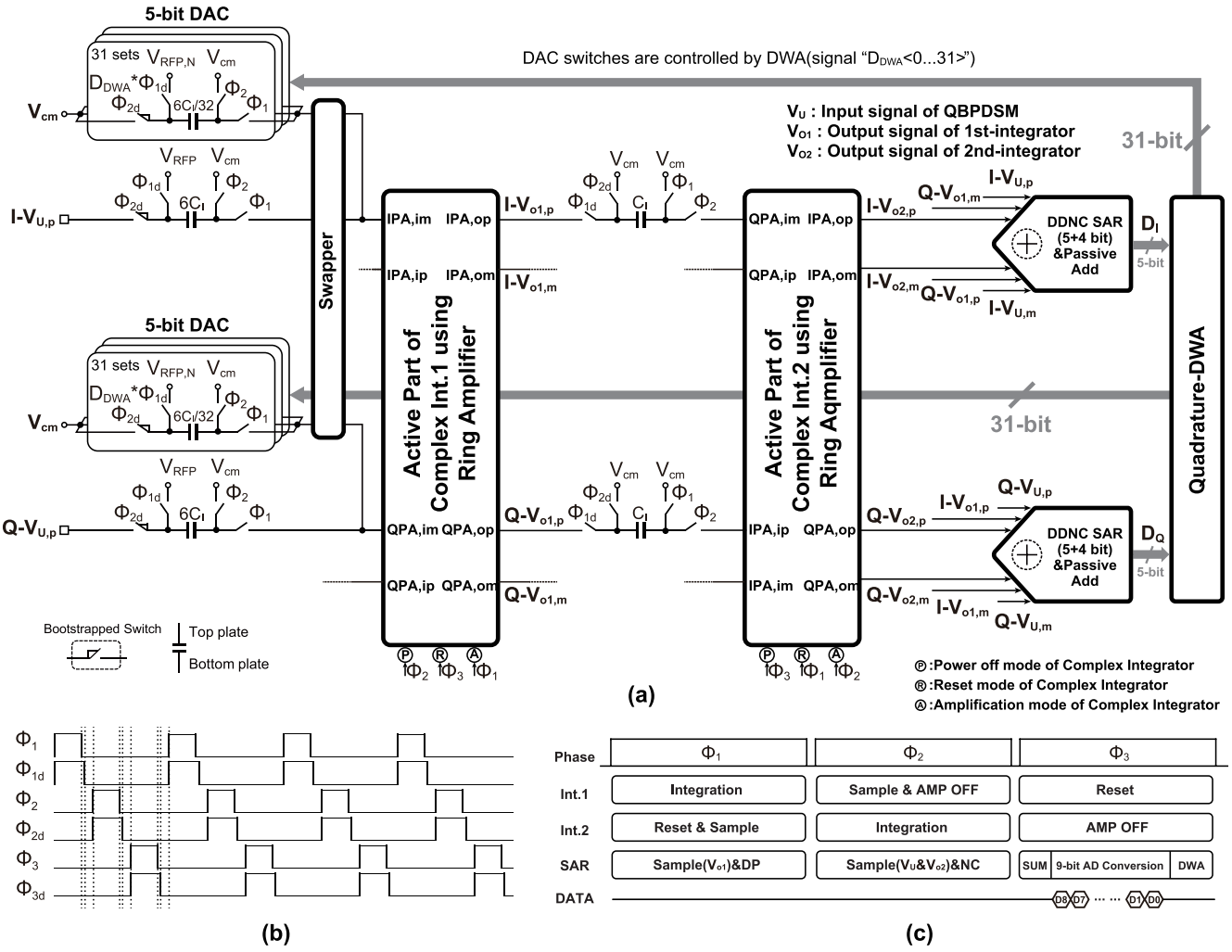

Fig. 2 Circuit implementation of the proposed 6th-order quadrature bandpass delta sigma AD modulator. (a) Circuit schematic diagram. (b) Clock timing chart. (c) Operation mode diagram.

improve the performance of QBPDSM, the noise coupling (NC) SAR quantizer is used for realizing high order noise shaping and image rejection. The SAR-assisted digital domain noise coupling technique can easily realize the high order noise shaping with maintaining the high energy efficiency, which is verified in pervious works [5]–[7]. In our work, the digital domain noise coupling technique is applied to the implementation of the NC SAR quantizer, moreover, a passive adder is embedded in the NC SAR quantizer to further improve the energy efficiency of the QBPDSM.

This paper proposed a 6th-order QBPDSM with 2nd-order image rejection using the dynamic-analog-components (ring-amplifier) based complex integrators and the digital domain noise coupling (DDNC) SAR quantizer. Two complex integrators consist of ring-amplifiers are used to realize the 2nd-order noise shaping. The passive adder embedded DDNC SAR quantizer is used to realize the analog adder in front of SAR quantizer, the quantization of input analog signal and the quantization noise coupling. Besides, the quantization noise is re-quantized, 4th-order digital shaped and re-injected to the delta sigma modulator, therefore, an additional 2nd-order noise shaping and 2nd-order image rejection is realized. SPICE simulations including the thermal noise and the flicker noise have been done to verify the effectiveness of the proposed architecture, and to confirm the performance of the QBPDSM. The peak SNDR of 76.30 dB is achieved while OSR=8 for sinusoid input at 8.33 MHz with −3.25 dBFS input amplitude.

This paper is structured as the following: Section 2 describes the architecture of the proposed QBPDSM. The implementation of the proposed QBPDSM is shown in Section 3. SPICE simulation results are presented in Section 4 to verify the effectiveness of the proposed QBPDSM. In the final section, the conclusion of this work is described.

2. Proposed Quadrature Bandpass DSM Architecture

Figure 1(a) shows the block diagram of the proposed QBPDSM which can realize the transfer function of

$$V(z) = U(z) + (1 - jz^{-1})^4(1 + jz^{-1})^2 Q(z) \quad (1)$$

where, V(z) is output signal, U(z) is input signal, Q(z) is

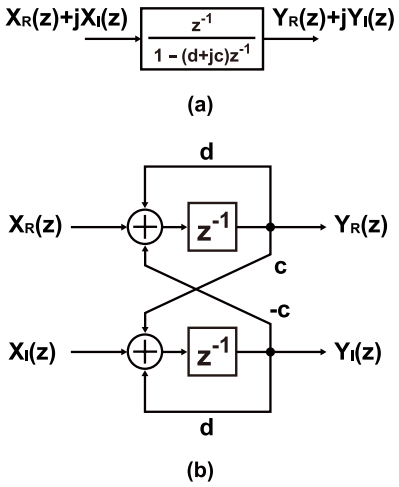

Fig. 3 Complex integrator. (a) Block diagram represented by transmission function. (b) Block diagram represented by delay.

quantization noise. The signal transfer function (STF) and noise transfer function (NTF) can be represented as

$$\mathrm{STF} = 1 \tag{2}$$

and

$$\mathrm{NTF} = (1 - jz^{-1})^4(1 + jz^{-1})^2, \tag{3}$$

respectively. It is consists of two complex integrators, two 5-bit DDNC SAR quantizers with passive adder, two DACs and a quadrature data-weighted-averaging (Q-DWA) logic. The proposed complex integrators using ring-amplifier are used to realize the 2nd-order noise shaping for reducing the circuit area and improving the energy efficiency of QBPDSM. The 5-bit passive adder embedded DDNC SAR quantizer is used to realize the summation of three analog input signals, quantization and noise shaping. The DDNC SAR quantizer is used not only as an internal quantizer, but also as a noise coupling circuit. As shown in Fig. 1(a), the quantization noise q(n) is converted to digital code by the internal 4-bit ADC, firstly. The digitized quantization noise q(n) is then processed by the digital filter with the transfer function of $-2z^{-2}-z^{-4}$. The output signal of the digital filter is finally coupled with the input signal of the DDNC SAR quantizer by the internal 6-bit DAC in the next period, so that, the FIR filtered quantization noise $(-2z^{-2} - z^{-4})q(n)$ is re-injected to the QBPDSM, which realize an addition 2nd-order noise shaping and 2nd-order image rejection. As a results, the proposed QBPDSM realizes 4th-order noise shaping and 2nd-order image rejection by using two complex integrators and the DDNC SAR quantizer as the Fig. 1(b). The zero points of proposed QBPDSM's noise transfer function ($z_1 = z_2 = z_3 = z_4 = +j$ and $z_5 = z_6 = -j$) are designed at the signal center frequency $f_{IR} = Fs/4$ and the image frequency $f_{IM} = 3Fs/4$, respectively. The noise caused by the mismatch of I, Q-paths in image frequency band is attenuated, so that, the noise reflected from image frequency band to desired signal band is suppressed, which can maintain the

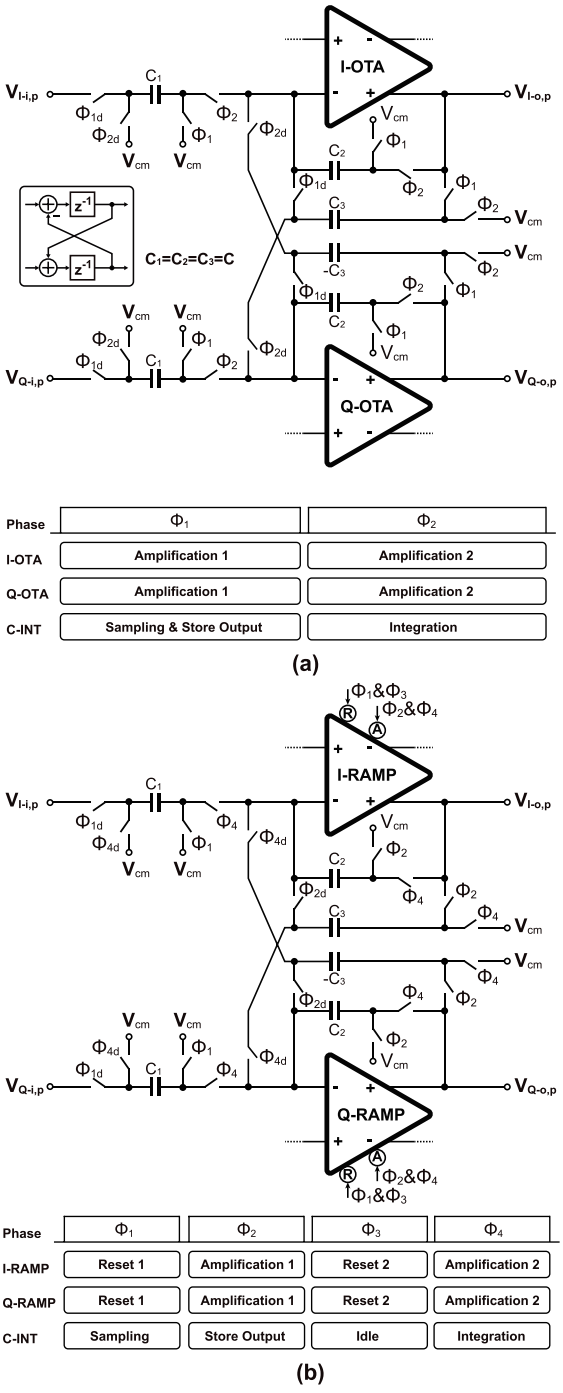

Fig. 4 Circuit implementation of complex integrator using the conventional method. (a) Circuit schematic and operation phase diagram of complex integrator using OTA. (b) Circuit schematic and operation phase diagram of complex integrator using RAMP (Ring-Amplifier).

high SNDR for the proposed QBPDSM. Moreover, the passive capacitor array instead of the active adder with a power hungry amplifier realizes the summation of analog signals in the front of DDNC SAR quantizer. Above techniques are conducted to improve the energy efficiency and to reduce the area of the proposed QBPDSM. The Quadrature-DWA circuit is also provided to the QBPDSM for suppressing the

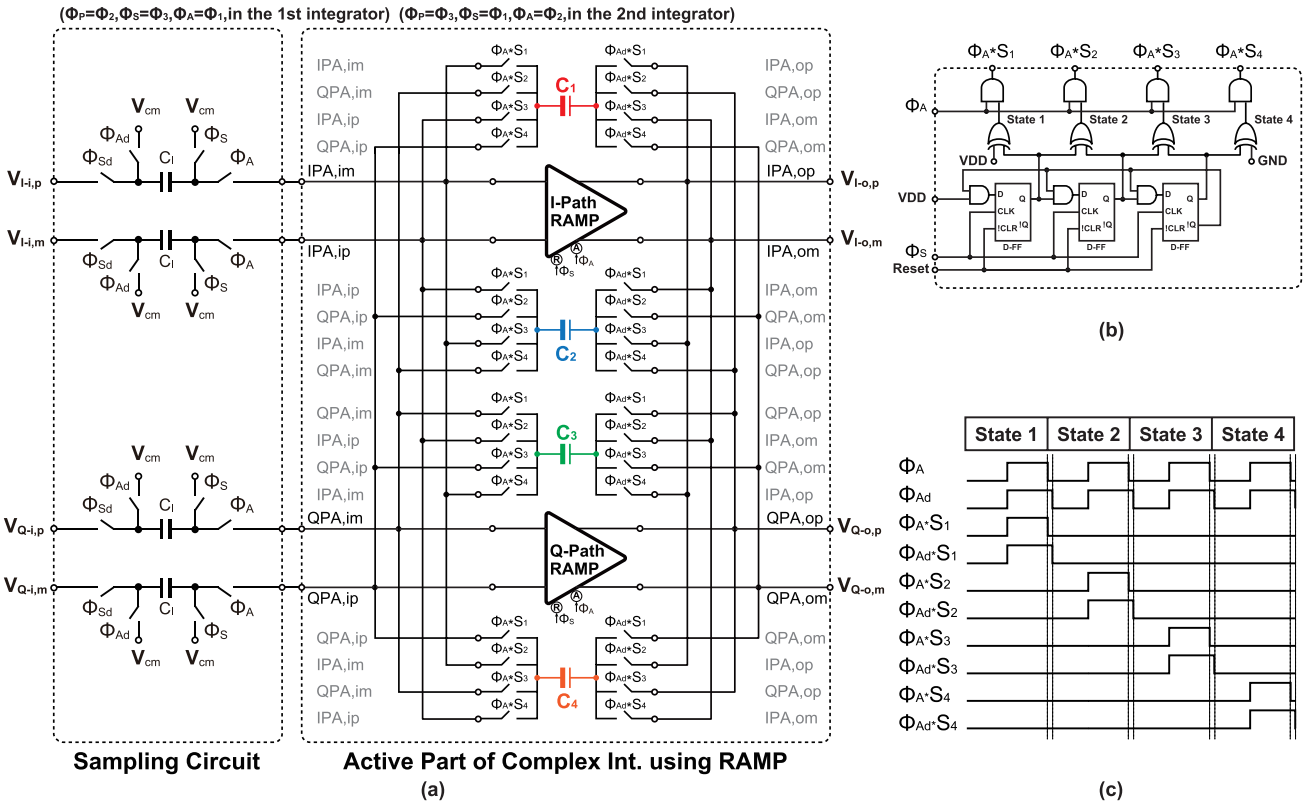

Fig. 5 Circuit implementation of the proposed complex integrator. (a) Circuit schematic diagram. (b) Switching controller circuit. (c) Control signals of switches.

influence of DAC mismatch.

3. Proposed Quadrature Bandpass DSM Implementation

Figure 2(a) illustrates the schematic diagram of the proposed 6th-order QBPDSM with two ring-amplifier based complex integrators and two passive adder embedded 5-bit DDNC SAR quantizers. Its clock timing chart and operation mode diagram are shown in Fig. 2(b) and Fig. 2(c), respectively. The proposed QBPDSM operates at 3 phases. During the phase Φ_1, the 1st-integrator performs the integration operation, the 2nd-integrator performs the sampling operation while the inside ring-amplifier is reset, and the output signals of 1st-integrator are sampled on the capacitors of the DDNC SAR quantizer. In addition, in the phase Φ_1, the digitized quantization noise of the previous period is also digital processed by the 4th-order FIR filter included in the DDNC SAR quantizer. During the phase Φ_2, the input signal of QBPDSM is sampled on the sampling capacitors of 1st-integrator and the DDNC SAR quantizer meanwhile, because the active part of 1st-integrator is idle, its power is cut off for maintaining the high energy efficiency. The 2nd-integrator performs the integration operation in the phase Φ_2, and the digital processed quantization noise is coupled to the QBPDSM at the same time for achieving the additional 2nd-order noise shaping and 2nd-order image rejection. During the phase Φ_3, the 1st-integrator is reset for the integration of the next period, the active part of 2nd-integrator is idle, so that its power is cut off, when the summation of 3 input analog signals is finished by the passive capacitor array, the DDNC SAR quantizer carry out the 9-bit AD conversion which include the 5-bit digital output signal and the 4-bit quantization noise.

In the proposed QBPDSM, the input signal of the QBPDSM and the output signal of 1st-integrator are fed to the DDNC SAR quantizer, which form the delta sigma modulator with the feed-forward architecture, hence, the signal input to the loop filter contains only the shaped quantization noise, the requirement of the slew-rate on the ring-amplifier can be relaxed, and the effect of amplifier's non-linearity can be reduced for the higher SNDR [4]. The proposed complex integrator using ring-amplifier shown in Fig. 5 can realize the complex integration by one phase, and it does not require the extra capacitors (C_3s shown in Fig. 4) for realizing the multiplication operation of the complex constant j, which is different from the conventional complex integrator. Therefore, not only the operation speed can be improved, but the circuit area can also be reduced. Moreover, the ring-amplifier can realize higher gain than the traditional amplifier at the low supply voltage, and the static current of the ring-amplifier is very small, so that it is suitable to achieve the QBPDSM with high energy efficiency. The 5-bit internal quantizer is realized by the SAR quantizer with digital domain noise coupling. It not only can improve the stability of the 6th-order QBPDSM, but also relax the require-

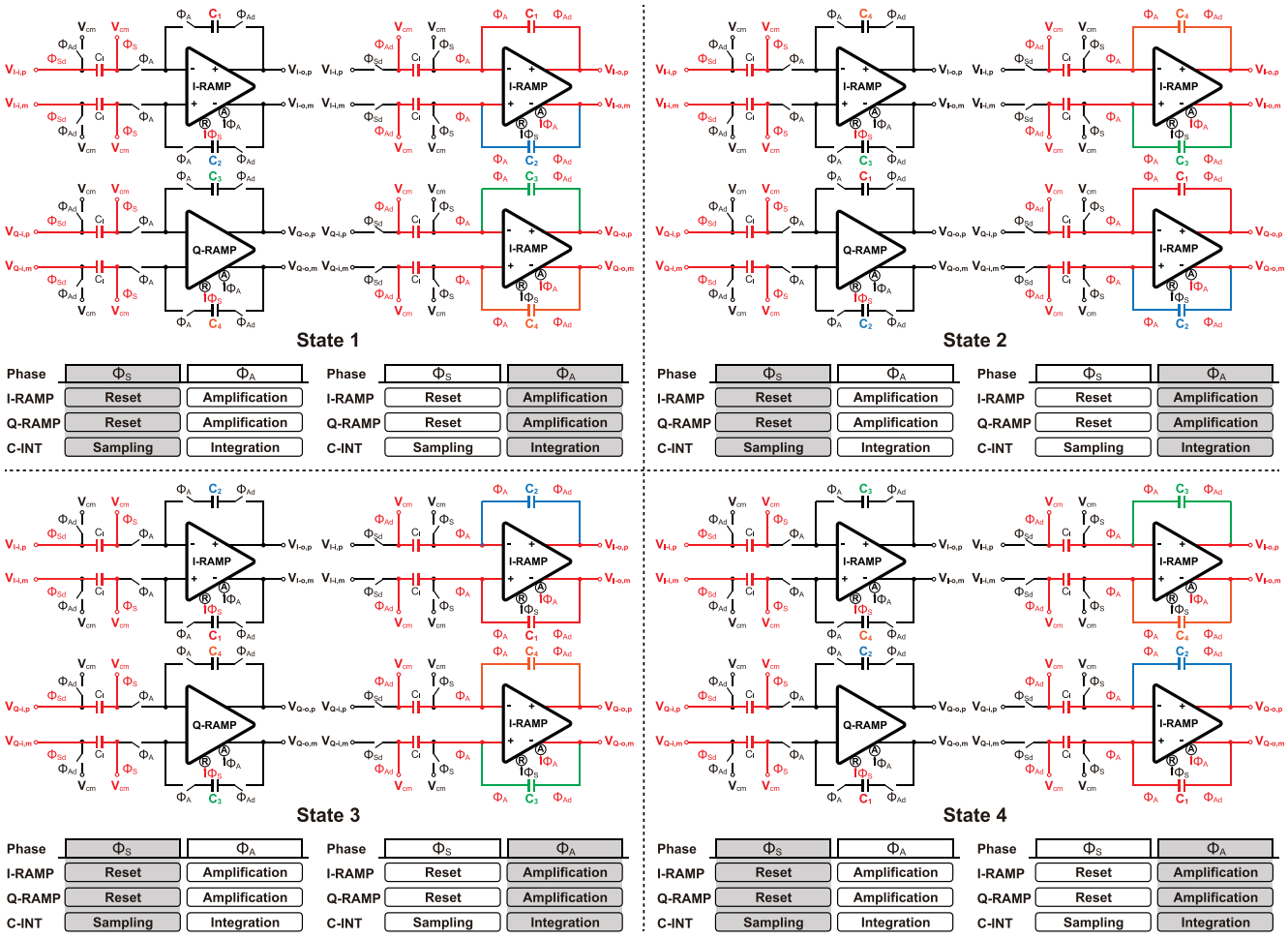

Fig. 6 Equivalent circuits of the proposed complex integrator in the four kinds of state.

ment on the slew-rate of amplifier in the complex integrator. Furthermore, the DDNC SAR quantizer can also couple the quantization noise of $(-2z^{-2}-z^{-4})q(n)$ shaped by digital signal process circuit for realizing an addition 2nd-order noise shaping and 2nd-order image rejection. The summation of 3 input signals (V_U, V_{o1} and V_{o2}) is realized by reconstituting the capacitor array of the DDNC SAR quantizer, thus, the analog adder with amplifier is not required. Two 5-bit capacitive DACs with the unit element shown in Fig. 2(a) are used for the feedback of the complex digital output signal of the QBPDSM. It is well known that the non-linearity caused by the capacitor mismatches of multi-bit DAC appears as the harmonic distortion which affect the SNDR of the QBPDSM. The Quadrature-DWA logic circuit [8] is used for reducing the influence of the DAC's non-linearity.

3.1 Proposed Complex Integrator Circuit

Figure 3(a) illustrates the block diagram of the complex integrator, it can also be represented by the delay circuit as shown in Fig. 3(b). The schematic diagram and the operation phase diagram of traditional complex integrator using OTA are shown in Fig. 4(a). The input signal is sampled on the capacitor C_1 during the phase Φ_1, and the charge stored on C_2 is transferred to C_3 at the same time. During the phase Φ_2, the summation of the charge on C_1 and C_3 is transferred to C_2 that achieve once complex integration operation. However, the amplifiers in the traditional complex integration circuit require to perform twice amplification actions for realizing once complex integration. Hence, two phases are required for performing once complex integration operation, which accompany the low power efficiency and the limited operation speed. In the traditional complex integrator using ring-amplifier circuit, the above defects will become worse. Due to the ring-amplifier requires the extra phase for the reset operation, four phases are required for performing once complex integration operation as shown in Fig. 4(b).

For solving the above problems, in this work, a novel implementation of the complex integrator using ring-amplifier is proposed as shown in Fig. 5(a). It is consists of the sampling circuit and the active part with ring-amplifier. The proposed complex integrator ($C_1 + C_2 + C_3 + C_4 = 4C$ in Fig. 5(a)) use the fewer capacitors compare with the traditional complex integrator ($((C_2 \times 2 + C_3 \times 2) \times 2$(differential circuit) $= 8C$ in Fig. 4) to achieve the inte-

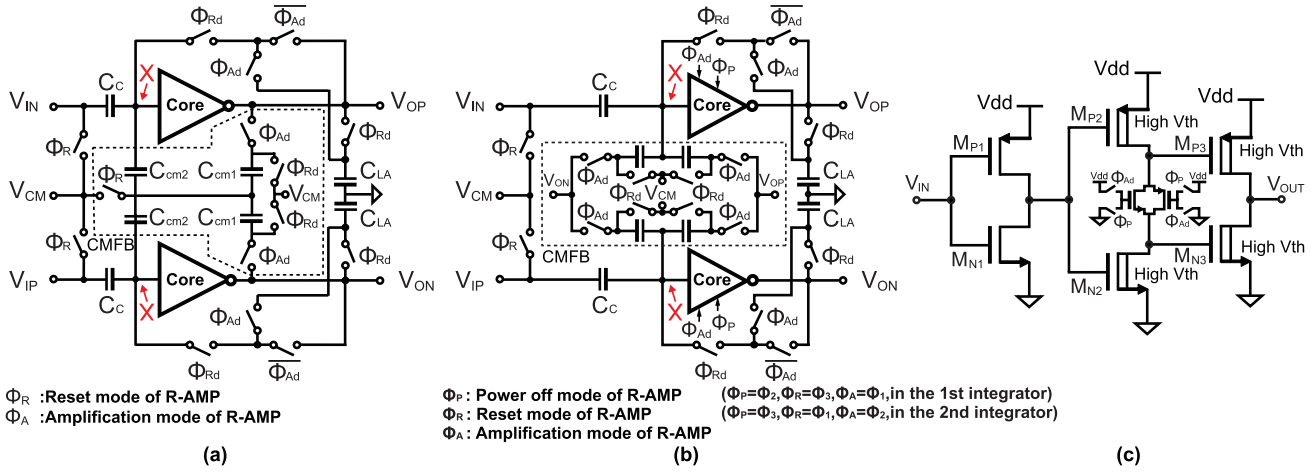

Fig. 7 Schematic of pseudo differential RAMP (Ring-Amplifier). (a) RAMP proposed in previous work. (b) RAMP proposed in this work. (c) Core of RAMP.

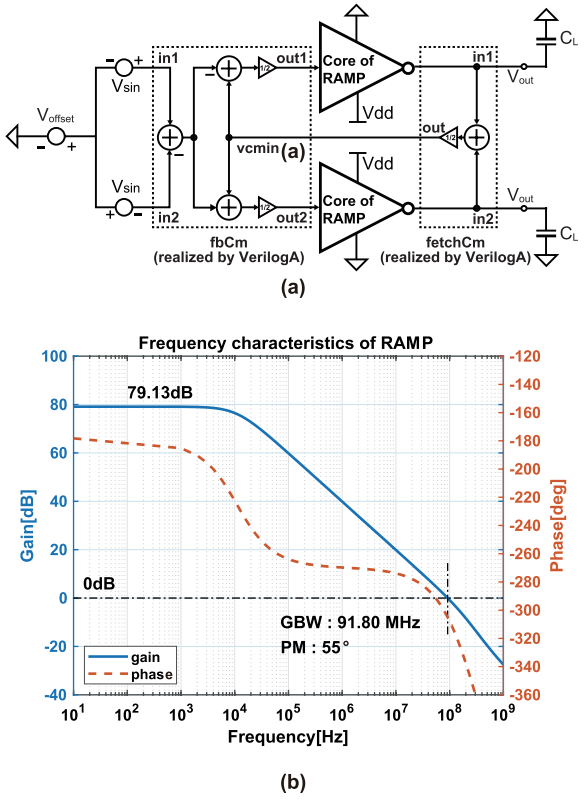

Fig. 8 AC analysis of RAMP (a) Simulation circuit. (b) Frequency characteristics RAMP.

gration operation of the complex signal, and only one amplification action is required for once complex integration. Thereby, the energy efficiency can be improved and the area of circuit can be reduced. Figure 5(c) shows the control signals of the active part, they are generated by the switching controller circuit shown in Fig. 5(b). By controlling the switches of the active part, the four kinds of states for the proposed complex integrator can be realized.

Figure 6 illustrates the equivalent circuits of complex integrator circuit in four kinds of the operation states. In the state-1, C_1, C_2 and C_3, C_4 are connected to the I-Path AMP and Q-Path AMP during Φ_A. When the integration operation is finished, the signals input to I-Path and Q-Path are stored on C_1, C_2 and C_3, C_4, respectively, as the state-1 shown in Fig. 6. In the next operation period, the complex integrator circuit become to state-2 by controlling the switches of active part. In the Q-Path channel, C_1 and C_2 are connected to the Q-Path AMP (they are connected to the I-Path AMP in the previous period), hence the signal input to I-Path in previous period (they are stored on C_1 and C_2 now) is added with the signal input to Q-Path in the current period. The result of summation is stored on the C_1 and C_2, which realize the additive operation from I-Path to Q-Path in Fig. 3(b). In the I-Path channel, the swapped C_3 and C_4 are connected to the I-Path AMP, so that the negative signal input to Q-Path in the previous period is added with the signal input to I-Path in the current period, the result of summation is stored on the C_3 and C_4 as the state-2 shown in Fig. 6, which realize the subtraction operation from Q-Path to I-Path in Fig. 3(b). As a results, the proposed complex integration circuit can realize the integration operation of complex signal by switching among four kinds of states continuously. It's different from a traditional complex integrator that only one amplification phase is required for achieving the complex integration operation, and the proposed complex integrator use the fewer capacitors than the traditional complex integrator shown in Fig. 4. Therefore, not only the high energy efficiency can be maintained, but the speed limit of QBPDSM can also be relaxed. Moreover, the use of the dynamic amplifier (ring-amplifier) instead of the OTA is used to achieve the maximum power-efficiency of the amplifier in the proposed complex integrator circuit.

3.2 Pseudo Differential Ring Amplifier

In this work, for maximizing the energy-efficiency of the proposed QBPDSM, we use the pseudo differential ring-

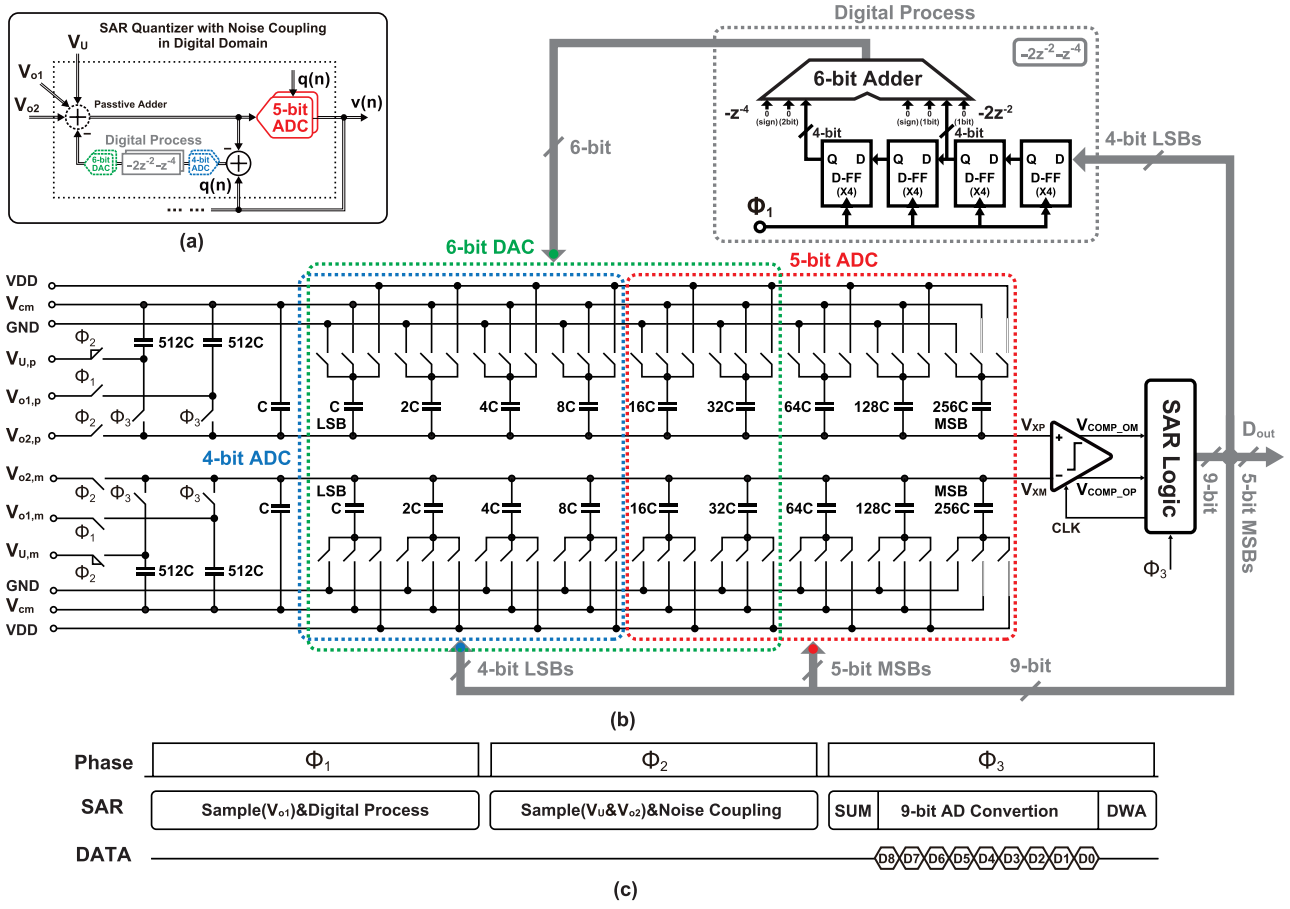

Fig. 9 Circuit implementation of proposed adder embedded SAR Quantizer with noise coupling in digital domain. (a) Block diagram. (b) Schematic diagram. (c) Clock timing chart.

amplifier to realize the complex integrator. The pseudo differential ring-amplifier is shown in Fig. 7. Its core circuit is consist of three inverters in series as shown in Fig. 7(c). Capacitors (C_C) are added to the input nodes of amplifier for saving the operation point of ring-amplifier. In the previous works [9] and [10], the common feedback circuit (CMFB) of pseudo differential ring-amplifier is consist of the capacitors C_{cm1}s and C_{cm2}s as shown in Fig. 7(a). C_{cm1}s are used for the detection of the output common voltage, C_{cm2}s are used for the feedback of the common voltage. Due to the C_C and C_{cm2} in series, the common voltage fed to the node "X" in front of core circuit can be represent as

$$V_{X\_common} = \frac{C_{cm2}}{C_{cm2} + C_C} \times V_{detected\_common}, \quad (4)$$

where $V_{detected\_common}$ is the common voltage detected at the output of ring-amplifier. Equation (4) means that the voltage division from the C_C and C_{cm2} causes the reduction of common mode rejection ratio (CMRR). This paper proposed the modified CMFB circuit as shown in Fig. 7(b). Because the modified CMFB circuit does not include the capacitors in series, it can feed directly the common mode signal detected at the output port of the ring-amplifier to the input port of the core circuit for obtaining the maximum CMRR. In the modified CMFB circuit, The detected common voltage is fed to node "X" (the input port of the core circuit), rather than is fed to input port of the ring-amplifier (V_{IN} and V_{IP}) as shown in Fig. 7(b), which can avoid that the virtual ground (input port of ring-amplifier) is affect by the common feedback circuit as same as the previous work [11]. When the feedback loop is formed in the input and output of ring-amplifier (eg. in amplification phase or reset phase), the voltage at the gate of the MOSFET M_{P1} and M_{N1} turns to V_{cm} during the steady state of the ring-amplifier. Thus, M_{P1} and M_{N1} operate in the weak inversion region at this time, which can achieve the high DC-gain with a very low static current as same as the class-AB amplifier. The transmission gate which used as a resistor is inserted at the output port of the 2nd-stage inverter, it can compress the drain-source voltages of M_{P2} and M_{N2} to the boundary between the weak and strong inversion regions for obtaining both wide GB bandwidth and high gain [12]. Moreover, it also establishes the different bias voltages at the gates of M_{P3} and M_{N3} to make the gate-source voltage lower than threshold voltage during the steady state. Therefore, the M_{P3} and M_{N3} behaves as push-pull structure which similar to a class-C amplifier for enhancing the slew-rate. In addition, by controlling the gate voltage of the transmission gate, the current of ring-amplifier's core can be broken in the

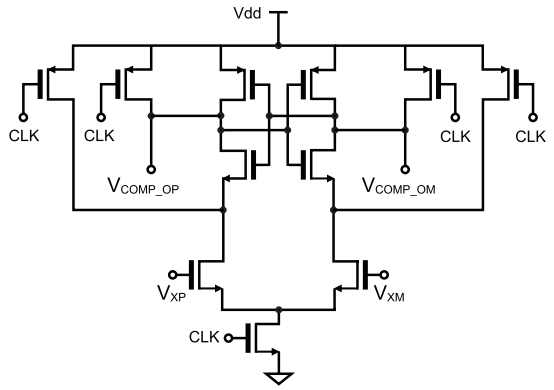

Fig. 10 Schematic diagram of dynamic comparator used in SAR ADC.

idle time to maximize the energy efficiency of QBPDSM.

In order to confirm the performance of ring-amplifier, the SPICE simulation of AC analysis using the circuit shown in Fig. 8(a) is introduced. In the simulation circuit, the common feedback circuits "fbCm" and "fetchCm" are realized by VerilogA program for obtaining the pure gain of ring-amplifier's core. The simulation results shown in Fig. 8(b) show that the ring-amplifier has DC-gain of 79 dB with 55° phase margin and unity-gain bandwidth of 91.8 MHz.

3.3 Noise Coupling SAR Quantizer

The block diagram and schematic diagram of the passive adder embedded noise coupling SAR quantizer are shown in Fig. 9(a) and Fig. 9(b), respectively. It consists of digital process circuit, capacitive DAC, a strong-ARM structure comparator (Fig. 10) and asynchronous SAR logic circuits. The clock timing chart is represented in Fig. 9(c). Figure 11(a)~(d) show the equivalent circuit of the DDNC SAR quantizer at four kinds of operation mode. In the sampling & digital process mode (Φ_1), the bottom plate of one capacitor among the DDNC SAR quantizer (512C) is connected to the output of the 1st integrator (V_{o1}). Meanwhile, the 4-bit digitized quantization noise is digital processed ($-2z^{-2} - z^{-4}$) as shown in Fig. 11(a). In the sampling & noise coupling mode (Φ_2), the bottom plate of another one capacitor among the DDNC SAR quantizer (512C) is connected to the input of the QBPDSM (V_U). The bottom plates of DDNC SAR quantizer's capacitors (512C) are connected to the output of the 2nd integrator (V_{o2}), the top plates of the 6-bit LSB capacitors for 6-bit DAC are connected to the reference voltage according to the output of the digital process circuit at the same time as shown in Fig. 11(b). Therefore, the shaped noise quantization $(-2z^{-2} - z^{-4})q(n)$ is coupled to the QBPDSM that can realize an addition 2nd-order noise shaping and 2nd-order image rejection. Moreover, because the capacitor ratio for three input signals is 1:1:1, the total charge stored on the capacitor Q_S can be expressed as $Q_S = 512C \times V_U + 512C \times V_{o1} + 512C \times V_{o2}$. In the summation mode Φ_3, the top plates of three sampled capacitors are connected to the input node of comparator (V_X) as shown in Fig. 11(c). Because the total capacitance at the node V_X is 1536C, the total charge Q_C of this summation mode on capacitors is $Q_C = 1536C \times V_X$. According to the charge-conservation law, we have $Q_C = Q_S$. Then, we get equation $V_X = Q_S/(1536C) = (V_U + V_{o1} + V_{o2})/3$, that means the summation of three input signals can be realized by capacitor array. After the analog input summation is finished, the AD conversion is carried out from MSB to LSB in the successive approximation manner as shown in Fig. 11(d). Asynchronous SAR logic circuits are used to control the capacitor DAC of DDNC SAR quantizer. As the result, the DDNC SAR quantizer not only realizes 5-bit quantization but also realizes an addition 2nd-order noise shaping and 2nd-order image rejection. Moreover, the active analog components are not required in the DDNC SAR quantizer, hence the high energy efficiency can be maintained.

3.4 Multi-Bit DAC and Quadrature-DWA Logic

Two 5-bit capacitor DACs are used for the 1st complex integrator as shown in Fig. 2(a), the mismatches among the unit elements in a multi-bit DAC cause the harmonic distortion in the signal band, the quadrature DWA logic circuit [8] is applied to the QBPDSM to reduce the influence of DAC non-linearity errors. The quadrature element rotation algorithm and an implementation of the Q-DWA logic are shown in the Fig. 12(a) and (b), respectively.

4. Simulation Results

The proposed 6th-order QBPDSM is designed in TSMC 90 nm CMOS technology. It operates at a clock rate of 33.3 MHz for a 2.083 MHz BW with an OSR of 8, and power consumption 6.74 mW under the supply voltage of 1.2 V for both analog circuit part and digital circuit part. Transistor-level SPICE simulations have been conducted to confirm the performance of the QBPDSM and to verify the effectiveness of the proposed architecture. The simulated spectrum results including single tone input signal (8.33 MHz with the amplitude of −3.25 dBFS), double tone input signals (8.19 MHz and 8.45 MHz with the amplitude of −9.27 dBFS) and the SNDR of the proposed QBPDSM are shown in Fig. 13. Figure 13(a) shows the simulated spectrum results without the thermal noise and the flicker noise. When the DWA circuit is disable, only SNDR of 24.44 dB and ENOB of 3.77 bit are achieved. When the DWA is applied, the SNDR and ENOB are improved to 89.99 dB and of 14.66 bit, respectively. In order to show the performance which close to the realistic circuit as much as possible, the simulated output signal spectrum shown in Fig. 13(b) includes the thermal noise, the flicker noise, the effect of $\leq$ 1% unit-capacitance mismatches of DAC, and the effect of non-ideal characteristic of circuit (eg. amplifier and comparator). The noise power and the non-ideal characteristic of transistor are calculated by simulator according to the transistor model of CMOS technology. In the simulation parameters, the maximum noise frequency is set as 100 MHz, it controls the bandwidth of energy which

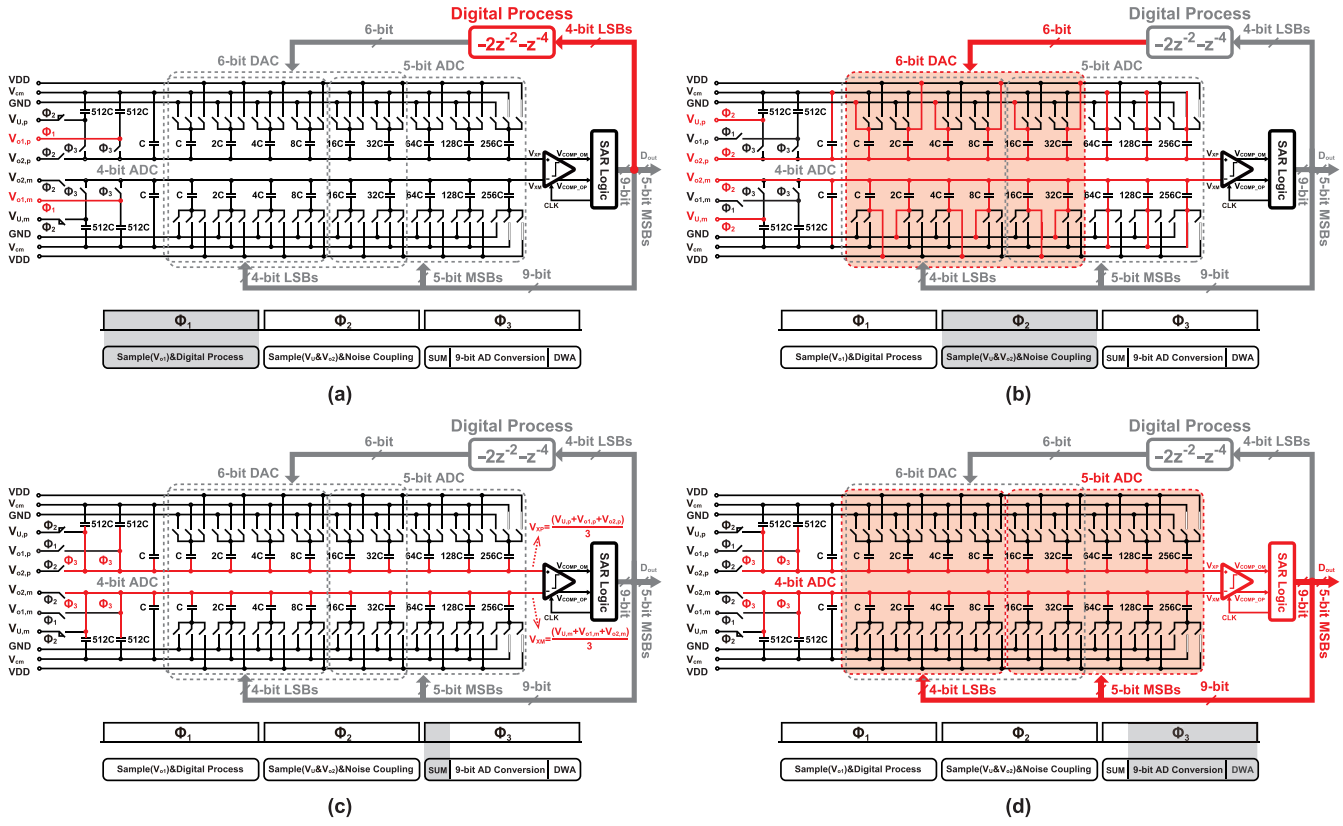

Fig. 11 Equivalent circuits of proposed adder embedded SAR Quantizer with noise coupling in digital domain. (a) Sampling & digital process mode. (b) Sampling & noise coupling mode. (c) Summation mode. (d) Successive approximation mode.

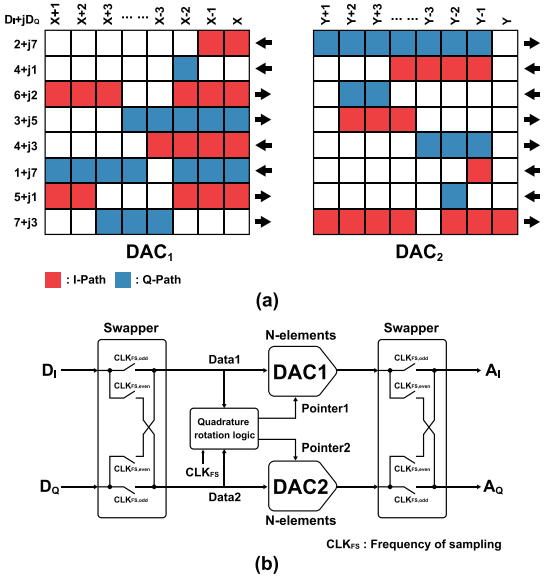

Fig. 12 Quadrature DWA logic. (a) Quadrature element rotation algorithm. (b) An implementation of the Q-DWA logic.

is emitted by the each noise source in the QBPDSM circuit. The minimum noise frequency is set as 10 KHz, it is used to establish the lower frequency bound on flicker noise modeling [13]. As shown in Fig. 13(b), When the DWA is disable, the peak SNDR of 24.38 dB and ENOB of 3.76 bit are achieved. When the DWA is applied, the SNDR and ENOB are improved to 76.30 dB and 12.38 bit, respectively. The simulated spectrum results shown in both of Fig. 13(a) and (b) also considered the effect of $\leq 1\%$ unit-capacitance random mismatches of DAC. Moreover, Fig. 13(c) and (d) shown the simulated spectrum results with double tone input signal, the IM3 of -117.74 dB is achieved when the thermal noise and the flicker noise is considered, which indicate that the distortion of proposed QBPDSM is acceptable. The performance of the QBPDSM is summarized in Table 1 in comparison with the previous works. The calculated FOMW and FOMS are 0.303 pJ/conversion-step and 161.2 dB respectively. Compared with the other works which have the similar signal bandwidth, the simulation results show that the proposed QBPDSM has a better energy efficiency (FOM). Although the noise and the non-ideal characteristic of circuit are considered in the simulation results, it is not the measurement the actual chip, the SNDR and FOM of the prototype modulator should be degraded from the SPICE simulation results. However, the operation speed and the signal bandwidth often meet the comparable value to the SPICE simulation results.

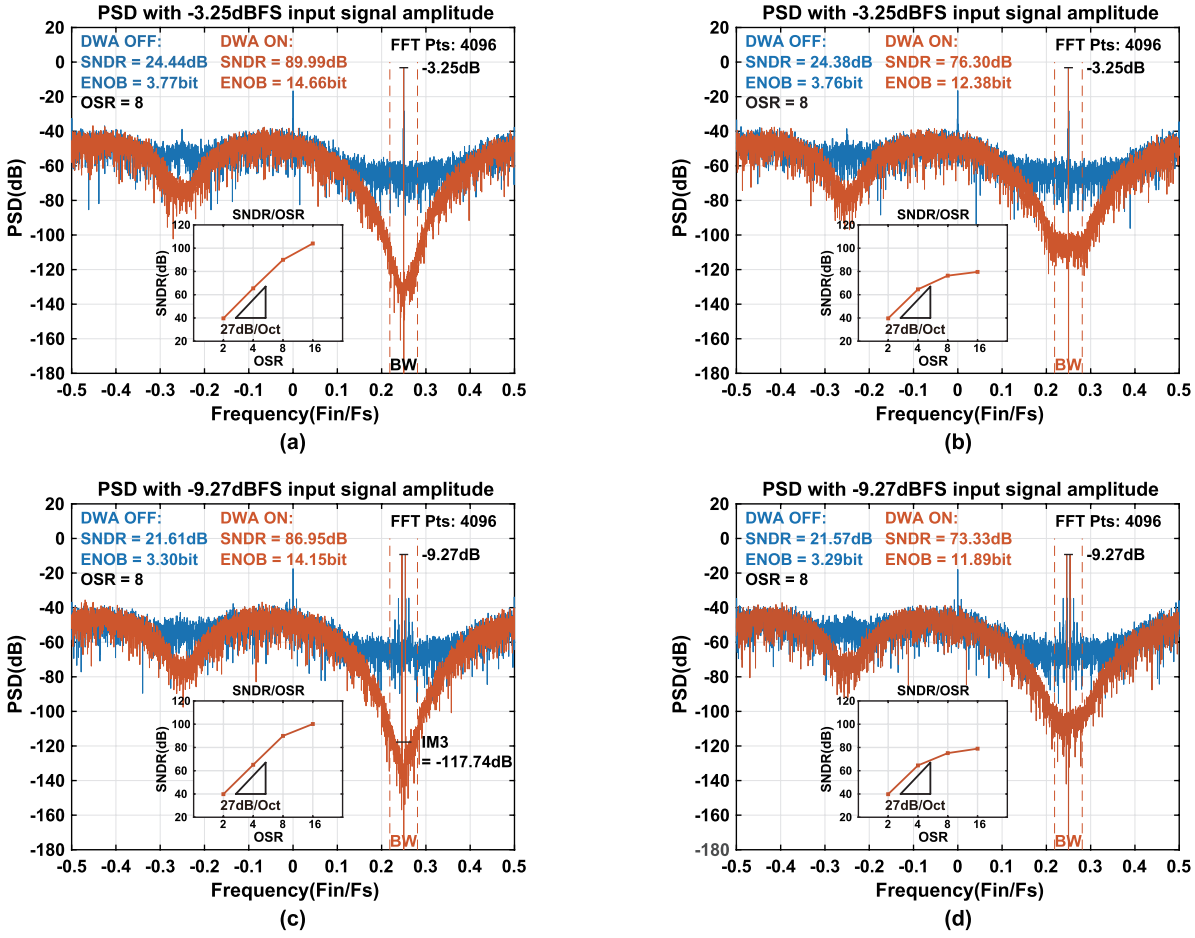

Fig. 13 Simulated output spectrum with ≤1% unit-capacitance mismatches of DAC for single tone (f_{in} ≈8.33 MHz with the input signal amplitude of −3.25 dBFS) and double tone (f_{in1} ≈8.19 MHz and f_{in2} ≈8.45 MHz with the input signal amplitude of −9.27 dBFS) (a) Single tone without thermal noise and flicker noise. (b) Single tone with thermal noise and flicker noise. (c) Double tone without thermal noise and flicker noise. (d) Double tone with thermal noise and flicker noise.

Table 1 Performance summary and comparison with previous works.

Specification	[14]	[15]	[16]	[17]	[18]	This work	
Technology(nm)	65	65	180	180	180	90	
Architecture	CT-4th	CT-2nd	CT-2nd	CT-4th	DT-2nd	DT-6th	
Supply voltage(V)	1.25	1.2	1.8	3.3	1.8	1.2	
Sampling rate (MS/s)	800	160	120	264	60	33.3	
OSR	16.7	16	12	15.5	30	8	
Signal BW (MHz)	24	5	5	8.5	1	2.083	
SNDR (dB)	58	65.9	61.2	77	65.1	89.99(N)	76.30(T)
Power (mW)	12	4.2	8.9	375	16	6.74	
FOMW (pJ/conv.-step)	0.385	0.261	0.949	3.805	5.441	0.06(N)	0.303(T)
FOMS (dB)	151	157	149	151	143	174.9(N)	161.2(T)

CT : Continuous time, DT : Discrete time
N : Without thermal noise and flicker noise
T : With thermal noise and flicker noise
FOMW = Power/$(2 \times \mathrm{BW} \times 2^{(\mathrm{SNDR}-1.76)/6.02})$
FOMS = SNDR + $10 \times \log_{10}(\mathrm{BW/Power})$

5. Conclusions

A 6th-order quadrature bandpass delta sigma AD modulator using dynamic amplifier and digital domain noise coupling SAR quantizer has been designed in 90 nm CMOS technology. A novel complex integrator circuit using ring-amplifier is proposed to improve the energy efficiency and to reduce the area of circuit. The proposed complex integrator only requires one amplification operation for the complex integration, so that the QBPDSM can operate at the high speed. Benefit from an additional 2nd-order noise shaping and the 2nd-order image rejection are realized by the digital domain noise coupling SAR quantizer, not only the bandwidth of the QBPDSM is extended, but also the influence of I,Q-path mismatch is reduced. Moreover, the digital signal process technique is used for the process of the quantization noise in the noise coupling SAR quantizer, the use of active analog component is not requited, thus the high energy efficiency is maintained. The simulation results show the feasibility of the proposed QBPDSM.

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