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A Noise Coupled ΔΣAD Modulator Using Passive Adder Embedded Noise Shaping SAR Quantizer

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SUMMARY   This paper presents a 3rd-order ΔΣAD modulator with noise coupling structure using the proposed passive adder embedded quantization noise shaping (QNS) SAR quantizer. QNS SAR quantizer can feedback shaped quantization noise and realize an additional 1st-order noise shaping by noise coupling technique. As a result, the 3rd-order noise coupled ΔΣAD modulator is realized by two integrators with ring amplifier and the QNS SAR quantizer. The SPICE simulation results demonstrate the feasibility of the proposed ΔΣAD modulator in 90nm CMOS technology. Simulated SNDR of 81.05dB is achieved while a sinusoid −4.32dBFS input is sampled at 100MS/s and the bandwidth is BW = 3.125MHz. The total power consumption in the modulator is 4.58mW while the supply voltage is 1.2V.
key words: *ΔΣAD modulator, SAR ADC, noise coupling*

1. Introduction

Wide band high resolution ADCs are widely used in the mixed-signal SoC in the fields of both the wireless communication system and the image sensor. SAR ADC is well known as an energy efficiency architecture for low and medium-speed, medium-resolution applications [1], [2]. Because the resolution of SAR ADC depends on the accuracy of capacitor matching and the offset of comparator, it is difficult to realize a high resolution SAR ADC in nanoscale CMOS technology. On the other hand, since the ΔΣAD modulator reduces the quantization noise in the desired signal band by oversampling and noise-shaping technique, it is suitable to realize the high SNDR ADC in nanometer CMOS technology [3]. The high SNDR modulator is realized by the techniques of high-order noise-shaping and/or higher oversampling ratio (OSR). However, high OSR needs high speed operation and increases the total power consumption of the modulator. Several techniques have been proposed to improve the SNDR and reduce the power consumption of the ΔΣAD modulator. Feed-forward architecture is used to reduce the output swing of the integrator, which can relax the linearity requirements on the amplifier in the integrator, and hence to reduce the power consumption of the ΔΣAD modulator. Error feedback technique (noise coupling) also has been proposed to aggressive the noise shaping characteristic of the ΔΣAD modulator [4]. Because SAR ADC have the worthy features that can hold

the quantization noise when the successive approximation is finished, the noise coupling technique realized by SAR ADC is proposed in recently published papers [5], [6]. The previously reported works [4] and [5] require the residue sampling and the active buffer circuit, that accompany the high power consumption. Although the digital domain noise coupling techniques can eliminate the drawbacks of analog domain noise coupling techniques, for realizing the requantization of quantization noise, a redundant 8-bit SAR ADC is used as the 4-bit internal quantizer [6]. It dissipates quantization ability of the internal quantizer of the ΔΣAD modulator (eg. the SQNR of 2nd ΔΣAD modulator with 8-bit internal quantizer is similar to the SQNR of 4th ΔΣAD modulator with 4-bit internal quantizer). In this work, an approach is proposed for realizing the quantization noise coupling, without the residue sampling circuit, the active buffer circuit and the redundant SAR ADC. The proposed noise coupling technique is realized in the analog domain, but it avoids the drawbacks of previous analog domain noise coupling techniques. Moreover, in order to achieve the maximum power-efficiency of the amplifier in ADC, the use of the dynamic amplifier (eg. logic inverter or ring amplifier) instead of the operational transconductance amplifier (OTA) has been proposed and thus results in dynamic-analog-components-based ADC [7], [8].

This paper proposes a 3rd-order noise coupled feedforward ΔΣAD modulator with two dynamic-analog-components-based integrators and a passive adder embedded QNS SAR quantizer. Two integrators consist of ring amplifiers are used to realize the 2nd-order noise shaping. The proposed passive adder embedded QNS SAR quantizer is used to realize analog signal summation, quantization and quantization noise shaping. The shaped quantization noise is re-injected to the modulator to realize an additional 1st-order noise shaping. The novel capacitor array architecture and control method are introduced to implement the proposed QNS SAR quantizer. SPICE simulations including
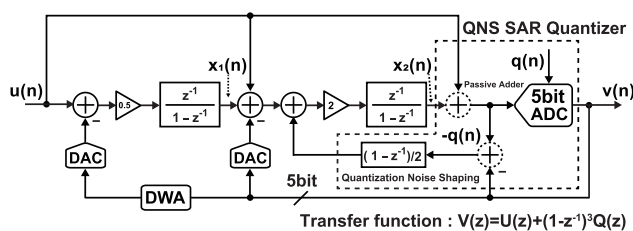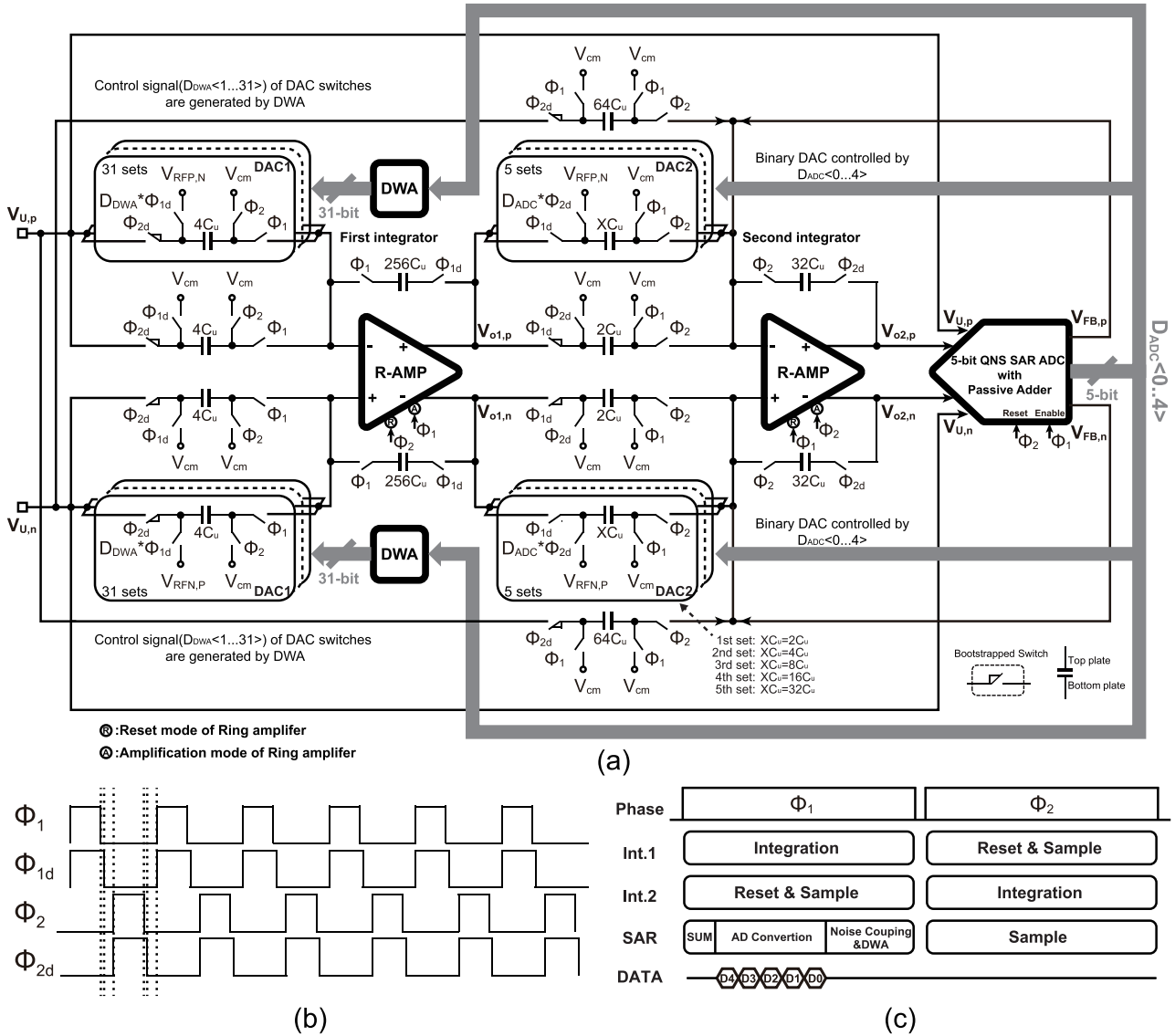
Fig. 1   Proposed architecture of ΔΣAD modulator.

Fig. 2 Circuit implementation of the proposed ΔΣAD modulator using ring amplifier (R-AMP) and passive adder embedded QNS SAR ADC. (a) Circuit schematic diagram. (b) Clock timing chart. (c) Operation mode diagram.

the thermal noise and the flicker noise have been done to verify the effectiveness of the proposed architecture and to confirm the performance of the modulator. The peak SNDR of 81.05dB is achieved while OSR = 16 for sinusoid input at 366.21kHz with −4.32dBFS input amplitude.

This paper is structured as the following: Section 2 describes the architecture of the proposed ΔΣAD modulator. The implementation of the proposed ΔΣAD modulator is shown in Sect. 3. SPICE simulation results are presented in Sect. 4 to verify the effectiveness of the proposed modulator. In the final section, the conclusion of this work is described.

2. Proposed ΔΣAD Modulator Architecture

Figure 1 shows the block diagram of the proposed 3rd-order ΔΣAD modulator. It consists of two integrators, a 5-bit

QNS SAR quantizer with passive adder, two DACs and data-weighted-averaging (DWA) logic. Two integrators are used to realize the 2nd-order noise shaping. The 5-bit passive adder embedded QNS SAR quantizer is used to realize analog signal summation, quantization and quantization noise shaping. The proposed QNS SAR quantizer is used not only as an internal quantizer, but also as a noise coupling circuit. The QNS circuit realizes the transfer function of $(1 - z^{-1})/2$ for quantization noise $-q(n)$ as shown in Fig. 1. The signal $-(1 - z^{-1})q(n)/2$ is transfered to the input node of the 2nd integrator, so that the quantization noise is re-injected to modulator for realizing an addition 1st-order noise shaping. Therefore, the noise coupled ΔΣAD modulator realizes 3rd-order noise shaping function by using two integrators. Moreover, the analog signal summation in front of SAR ADC is realized by the passive circuit instead of the active
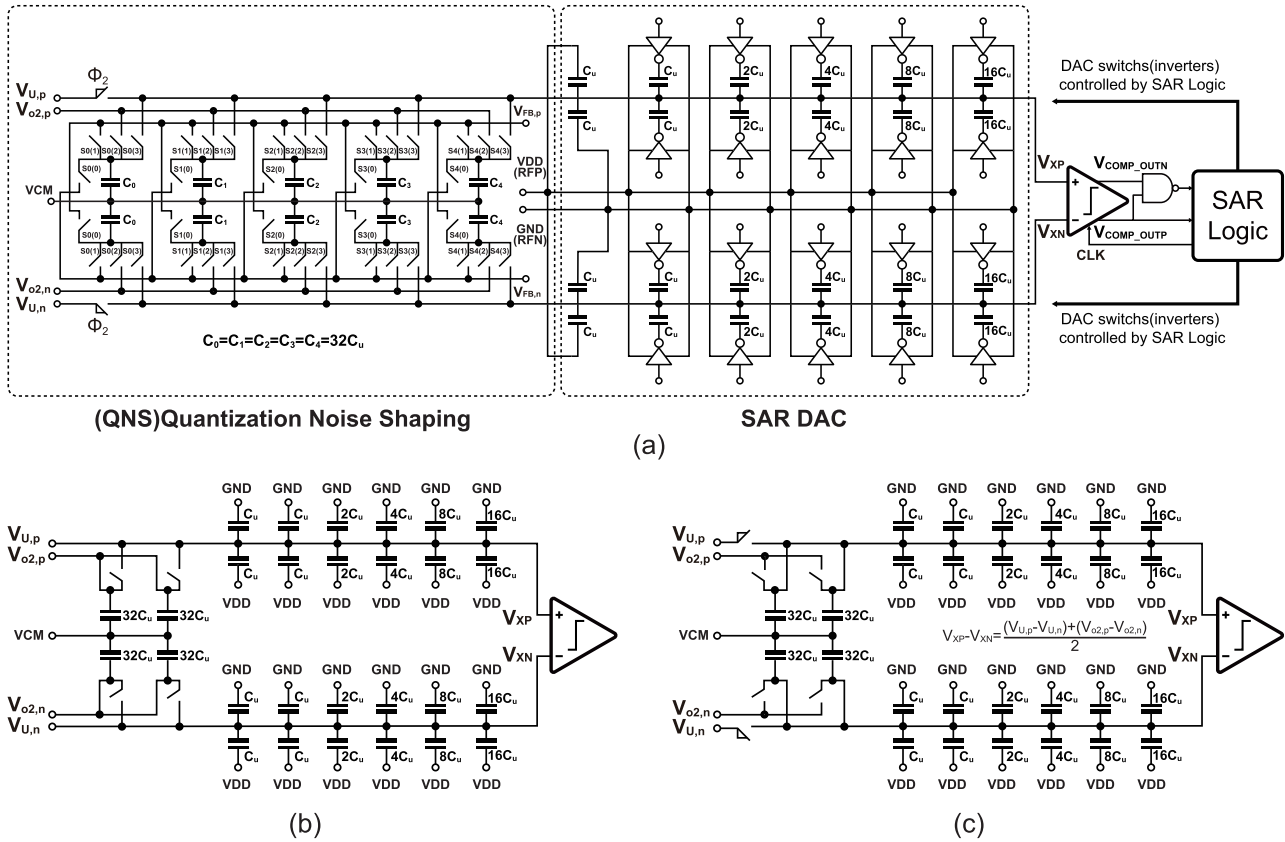
Fig. 3 Circuit implementation of proposed passive adder embedded QNS SAR Quantizer. (a) Schematic diagram of the SAR ADC. (b) Equivalent circuit of the SAR ADC at the sampling mode. (c) Equivalent circuit of the SAR ADC at the summation and successive approximation mode.

adder with a power hungry amplifier. Above techniques are conducted to reduce the active area and power dissipation of the proposed ΔΣAD modulator. The DWA technique is also provided to the modulator for suppressing the influence of DAC mismatch.

3. Proposed ΔΣAD Modulator Implementation

Figure 2 (a) illustrates the schematic diagram of the proposed 3rd-order ΔΣAD modulator with two ring-amplifier-based integrators and a 5-bit QNS SAR quantizer with passive adder. Its clock timing chart and operation mode diagram are shown in Fig. 2 (b) and Fig. 2 (c), respectively. The proposed ΔΣAD modulator is the feed-forward architecture, and the input signal to the loop filter contains only the shaped quantization noise, so that the modulator can reduce the influence of amplifier's non-linearity for higher SNDR [9]. The ring amplifier for the integrators can realize higher gain than the traditional amplifier at low supply voltage, and the static current of the ring amplifier is very small, so that the power consumption of the modulator can be maintained low. The 5-bit QNS SAR ADC is used as a multi-bit quantizer in the modulator, not only the stability of the 3rd-order modulator is improved, but also the requirement on the slew-rate of amplifier is relaxed. In addition, the quantizer can also feedback the signal containing the quanti-

zation noise of $-(1-z^{-1})q(n)/2$ for realizing noise coupling. The 5-bit QNS SAR ADC has 2 inputs terminal (V_U and V_{o2}), since the quantizer converts the summation of them to digital code by passive capacitor, the analog adder with amplifier is not necessary. A 5-bit capacitive DAC (DAC1) with unit-segment-element in Fig. 2 (a) is used for the 1st integrator. While the capacitor mismatches among the unit elements in a multi-bit DAC cause the harmonic distortion in the signal band, the DWA logic circuit [11] is applied to reduce the influence of DAC nonlinearity errors. Although the noise caused by the capacitor mismatch of DAC2 is injected into the ΔΣAD modulator from the input of the 2nd integrator, the non-linear noise is 1st-order shaped by the 1st integrator. Therefore, the 5-bit capacitive DAC (DAC2) in Fig. 2 (a) for the 2nd integrator is designed as a binary-weighted-element without DWA for simplicity.

3.1 Passive Adder Embedded QNS SAR Quantizer

Figure 3 (a) shows the schematic diagram of the proposed passive adder embedded QNS SAR quantizer. It consists of QNS circuit, capacitive DAC, a dynamic comparator (Fig. 5) and asynchronous SAR logic circuits. Figure 3 (b) and Fig. 3 (c) show the equivalent circuit of capacitor array as the passive adder at two kinds of operation mode. Note that the QNS circuit consists of five parts of capacitors
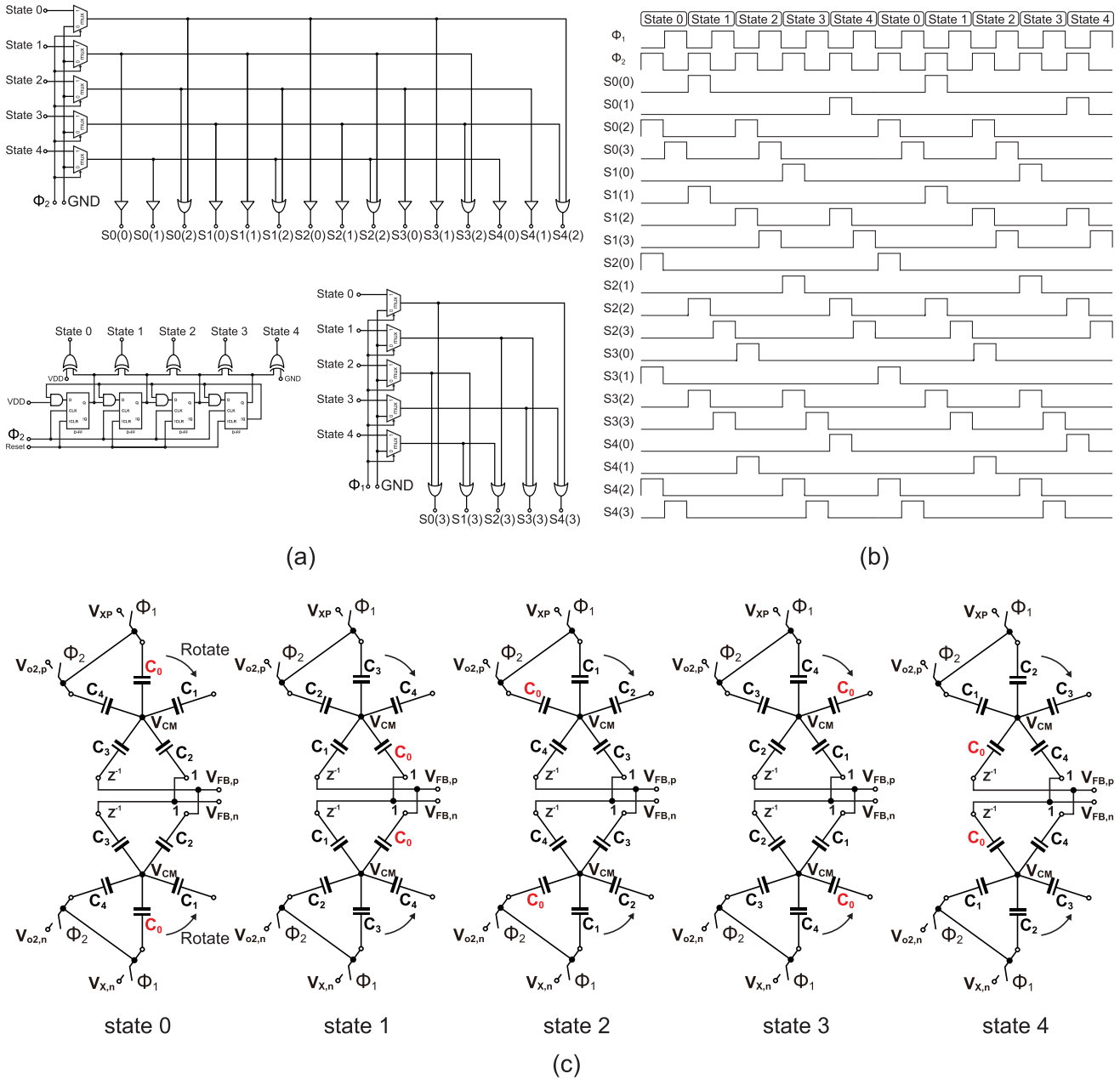
Fig. 4 Circuit implementation of proposed the QNS circuit. (a) Clock generator of the QNS circuit. (b) Clock timing chart of the QNS circuit. (c) Equivalent circuits of the five kinds of the QNS circuit's state.

which have the same capacitance ($32C_u$). In the sampling mode (Φ_2), the bottom plates of two capacitors among the QNS circuit's capacitors ($64C_u$) are connected to the output of the 2nd integrator (V_{o2}). Meanwhile, the top plates of SAR DAC's capacitors ($64C_u$) are connected to the input of the ΔΣAD modulator (V_U) as shown in Fig. 3 (b). The capacitor ratio for 2 input signals is 1 : 1, then the total charge stored on the capacitor Q_s can be expressed as $Q_S = 64C_u \times V_U + 64C_u \times V_{o2}$. In the summation mode (Φ_1), the bottom plates of two sampled capacitors are connected to the input node of comparator (V_X) as shown in Fig. 3 (c). Because the total capacitance at the node V_X is

$128C_u$, the total charge Q_C of this summation mode on capacitors is $Q_C = 128C_u \times V_X$. According to the charge-conservation law, we have $Q_C = Q_S$. Then, we get equation $V_X = Q_S/(128C_u) = (V_U + V_{o2})/2$, that means the summation of 2 input signals can be realized by capacitor array. After the analog input summation is finished, the AD conversion is carried out from MSB to LSB in the successive approximation manner.

When the successive approximation is finished, the voltage of comparator's input node V_X equals to the half of negative quantization noise $-q(n)/2$, and the residual voltage is stored on the two capacitors used for sampling among
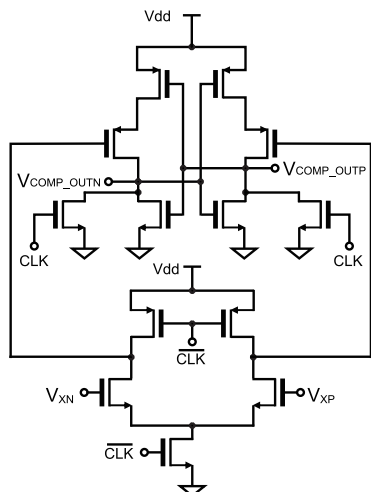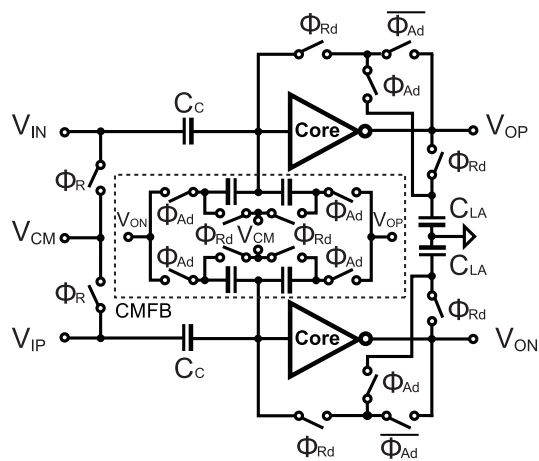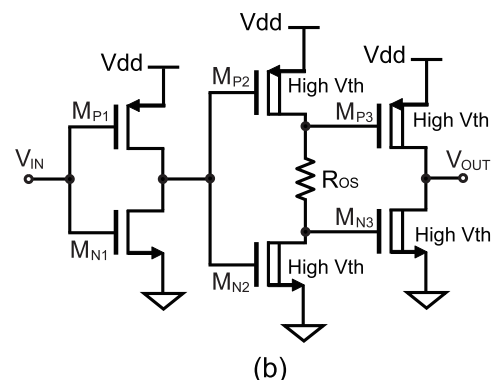
Fig. 5 Schematic diagram of dynamic comparator used in QNS SAR ADC.

Φ_R : Reset mode of R-AMP
Φ_A : Amplification mode of R-AMP
($\Phi_R=\Phi_2,\Phi_A=\Phi_1$,in the 1st integrator)
($\Phi_R=\Phi_1,\Phi_A=\Phi_2$,in the 2nd integrator)

(a)

(b)

Fig. 6 Schematic of pseudo differential R-AMP (a) R-AMP (Ring-Amplifier). (b) Core of R-AMP.

the 5 capacitors in QNS circuit. Moreover, the QNS circuit not only save the the residual voltage of quantization noise, but also realize the transfer function $(1 - z^{-1})/2$ by controlling the switches of the QNS circuit. Figure 4 (a) illustrates the schematic diagram of the clock generator for the QNS circuit. S0(0) to S4(3) shown in Fig. 4 (b) are control signals for the switches of QNS circuit as shown in Fig. 3 (a), it realizes the five kinds of QNS circuit's operation states. Figure 4 (c) illustrates the equivalent circuits of the QNS circuit in five kinds of the operation states. In the state 0, C_0 and C_4 are used for sampling during Φ_2 and passive addition during Φ_1. When the successive approximation of the quantizer is finished, $-q(n)/2$ is stored on C_0 and C_4. In the next operation period, the QNS circuit become to state 1 by rotating the capacitors around the midpoint, C_3 and C_2 are used for the sampling during Φ_2 and passive addition during Φ_1. C_0 is connected to V_{FB} that can realize $-q(n)/2$. Meanwhile, C_1 with the quantization noise of the previous period is connected to V_{FB} which can realize $-z^{-1}(-q(n)/2)$. As the result, the QNS circuit is rotated among five kinds of state continuously, and the noise signal $(1 - z^{-1})(-q(n))/2$ is outputted from the terminal of the QNS circuit V_{FB}. The signal V_{FB} is connected to the input node of the 2nd integrator that realize an extra 1st-order noise shaping by our proposed noise coupling technique. Therefore, the 3rd-order noise shaping characteristics is realized only with two dynamic amplifiers (ring amplifier), thus the power consumption can be kept at a low level in the proposed $\Delta\Sigma$AD modulator. Moreover, since the capacitors of the QNS circuit are used for sampling and feedback in the rotated manner at each period, as the same as the DWA manner, the capacitors mismatch of $(C_0 \ldots C_4)$ in the QNS circuit can also be shaped. Asynchronous SAR logic circuits [18] are used to control the capacitor DAC of 5-bit SAR quantizer. The operation speed of the asynchronous SAR logic circuit may be reduced at the PVT worst case. Since the required operation time of asynchronous SAR logic circuit in our modu-

lator can be drastically relaxed than a high speed ADC, the speed reduction of SAR logic circuit can considered have no significant influence on the proposed QNS SAR quantizer. Moreover, the proposed quantization noise coupling technique is not requite using the active analog component, the lower power consumption can be maintained.

3.2 Pseudo Differential Ring Amplifier

In this work, we use the pseudo differential ring amplifier proposed in the previous work [8], [10] to realize the integrator for achieving the maximum power-efficiency of the amplifier in the $\Delta\Sigma$AD modulator. Figure 6 (a) shows the pseudo differential ring amplifier. Capacitors (C_C) are added to the input nodes of amplifier to realize the amplifier input offset cancellation for the integrator. In the previous works [8] and [10], the voltage division from the C_C and the capacitors of the common mode feedback (CMFB) circuit cause the reduction of common mode rejection ratio (CMRR). This paper proposes the modifying CMFB circuit as shown in Fig. 6 (a). Because the CMFB circuit not in-

clude capacitors in series, it can directly feedback the common mode signal from the output terminal of the ring amplifier's core to the input terminal of the ring amplifier's core for obtaining the maximum CMRR. The core of ring amplifier is shown in Fig. 6 (b). It is constructed with three stage cascaded inverters. The input of the MOSFET M_{P1} and M_{N1} are biased at V_{cm} when the ring amplifier forms a feedback loop, therefore, the M_{P1} and M_{N1} operate in the weak inversion region during the steady state of the amplifier with a very low static current. The inverter which consists of M_{P1} and M_{N1} behaves as a class-AB amplifier providing high DC-gain and good linearity. The R_{OS} can compress the drain-source voltage of the M_{P2} and M_{N2} to the boundary between the weak and strong inversion regions for obtaining both high DC-gain and wide GB [7]. In addition, it also generates the different offset voltages to the gate of M_{P3} and M_{N3} for setting their gate-source voltage at lower than threshold. Therefore, the push-pull inverter consisting of M_{P3} and M_{N3} behaves as a class-C amplifier for reducing the setting time of the ring amplifier dramatically.

3.3 Multi-bit DAC and DWA Logic Circuit

A 5-bit capacitor DAC is used for the 1st integrator as shown in Fig. 2, the mismatches among the unit elements in a multi-bit DAC cause the harmonic distortion in the signal band, the data-weighted-averaging (DWA) logic circuit [11] is applied to the ΔΣAD modulator to reduce the influence of DAC non-linearity errors. To illustrate the effect of the DWA logic circuit, the Monte Carlo analysis comparison with the proposed modulator is performed by MATLAB in 2 cases: (a) 4-bit DAC with ≤ 1% unit-capacitance random mismatches while DWA at ON mode; (b) 4-bit DAC with ≤ 1% unit-capacitance random mismatches while DWA at OFF mode. Analyzed results of the above 2 cases are shown in Fig. 7 (a) and (b), respectively. While the unit-capacitance of DAC is variated without DWA, the non-linearities of DAC raise the in-band noise floor, and cause the harmonic distortion,
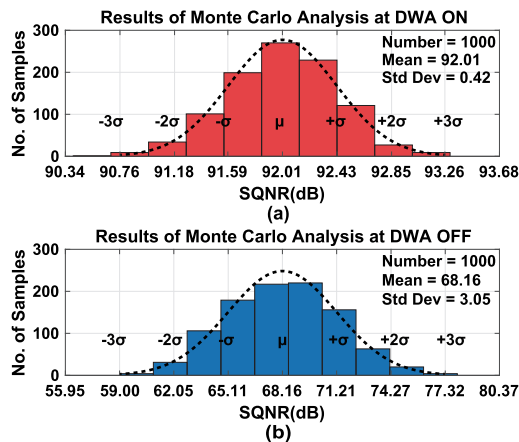
the average SQNR of 68.16dB is shown in Fig. 7 (b). On the other hand, while DWA technique is applied, the in-band noise and the harmonic distortion in the signal band are noise-shaped, the average SQNR reaches 92.01dB as shown in Fig. 7 (a).

4. Simulation Results

The proposed 3rd-order ΔΣAD modulator is designed in TSMC 90nm CMOS technology. The proposed ΔΣAD modulator operates at a clock rate of 100MHz for a 3.125MHz BW with an OSR of 16, and power consumes 4.58mW under supply voltage of 1.2V for both analog circuit part and digital circuit part. Transistor-level SPICE simulations have been conducted to confirm the performance of the modulator and to verify the effectiveness of the proposed architecture. The simulated spectrum results with a −4.32dBFS 366.21kHz sine signal and the SNDR of the proposed modulator are shown in Fig. 8. Figure 8 (a) shows the simulated spectrum result without the thermal noise and the flicker noise. When the DWA is not applied, the only peak SNDR of 70.59dB and SFDR of 71.74dB are achieved. When the DWA is applied, the SNDR and SFDR are im-
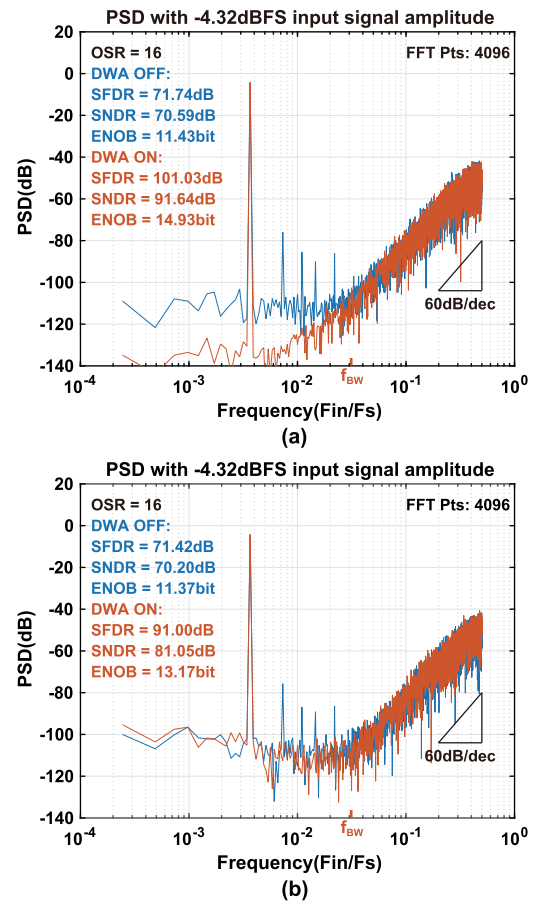
Fig. 8 Simulated output spectrum with ≤1% unit-capacitance mismatches of DAC for f_{in} ≈ 366.21kHz and −4.32dBFS input signal amplitude. (a) without thermal noise and flicker noise. (b) with thermal noise and flicker noise.

Fig. 7 Monte carlo analysis results comparison of ΔΣAD modulator performed by matlab with ≤1% unit-capacitance random mismatches of DAC. (a) DWA ON. (b) DWA OFF.

Table 1   Performance summary and comparison with previous works

Specification	[6]***	[5]***	[17]***	[16]***	[15]*	[14]*	[13]**	This work	
Technology (nm)	28	65	55	180	90	90	90	90	
Architecture	CT-4th	CT-6th	CT-4th	DT-3rd	DT-2nd	DT-3rd	DT-3rd	DT-3rd	
Supply voltag e(V)	1.1/1.2	1.8	1.2/1.8	1.2	1.2	1.2	1.2	1.2	
Sampling rate (MS/s)	320	900	140	25	60	80	60	100	
OSR	16	10	32	8	15	16	16	16	
Signal BW (MHz)	10	45	2.2	1.56	2	2.5	1.875	3.125	
SNDR (dB)	74.4	75.3	90.4	75	56	81.97	78.8	91.64 (N)	81.05 (T)
Power (mW)	4.2	24.7	4.5	2.6 (A)	1.56	2.53 (A)	1.59 (A)	3.49 (A)	
				3.75 (D)		1.64 (D)	1.26 (D)	1.09 (D)	
FOMW (fJ/conv.-step)	49.3	57.7	37.8	442.1	756.5	81.5	95.2	23.4 (N)	79.4 (T)
FOMS (dB)	168.1	167.9	177.3	158.9	147.1	169.7	168.0	179.9 (N)	169.4 (T)

***: Experimental results with thermal noise, **: Post-layout simulation results without thermal noise, *: Transistor-level simulation results without thermal noise
A: Analog, D: Digital, N: Without thermal noise and flicker noise, T: With thermal noise and flicker noise
$FOMW = Power/(2 \times BW \times 2^{(SNDR-1.76)/6.02})$
$FOMS = SNDR + 10 \times \log_{10}(BW/Power)$
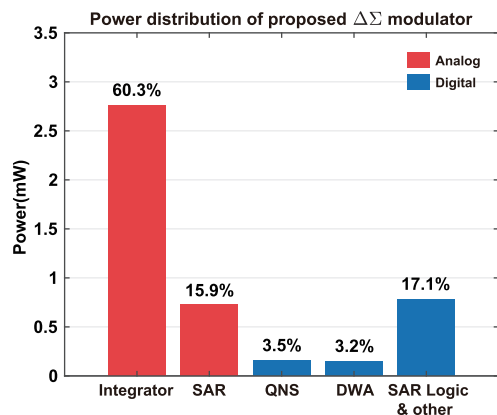
Fig. 9   Power distribution of proposed $\Delta\Sigma$AD modulator.

proved to 91.64dB and of 101.03dB, respectively. In order to show close to the measured performance of the $\Delta\Sigma$AD modulator as much as possible, the simulation including both thermal noise and flicker noise calculated by the SPICE simulator according to the CMOS process library model is performed. The maximum noise frequency parameter of the simulator is set as the clock rate of 100MHz, it controls the amount of energy each noise source can emit. The minimum noise frequency parameter of the simulator is set as 10KHz, it establishes the lower frequency bound on flicker noise modeling [12]. Figure 8 (b) shows the simulated spectrum result including thermal noise and flicker noise. When the DWA is not applied, the peak SNDR of 70.20dB and SFDR of 71.42dB are achieved. When the DWA is applied, the SNDR and SFDR are improved to 81.05dB and 91.00dB, respectively. Moreover, the simulated spectrum results shown in both of Fig. 8 (a) and (b) also considered the affect of $\leq 1\%$ unit-capacitance random mismatches of DAC. Figure 9 illustrates the percentage of power consumption for each module: the integrators about 60.3% of the total power; the SAR quantizer about 15.9%; the QNS control circuit about 3.5%; the DWA circuit about 3.2%; and the

other digital circuit, including the SAR logic circuit, DAC control circuit and the clock buffer about 17.1%.

The performance of the proposed $\Delta\Sigma$AD modulator is summarized in Table 1 in comparison with the previous works. The operation speed and the signal band width are comparable to other works. The calculated FOMW and FOMS are 79.4fJ/conversion-step and 169.4dB respectively. Compared with other similar BW work, the simulations show an better FOM. Although the influence of thermal noise, flicker noise and cap-mismatch are considered in the simulation results of proposed $\Delta\Sigma$AD modulator, it is not a chip's measurement, the SNDR and FOM of the prototype modulator should be degraded from the SPICE simulation results. However, the operation speed and the signal band width often meet the comparable value to the SPICE simulation results.

5.   Conclusions

A 3rd-order $\Delta\Sigma$AD modulator with noise coupling technique using passive adder embedded quantization noise shaping (QNS) SAR quantizer has been designed in 90nm CMOS technology. Benefit from the quantization noise feedback function of the proposed QNS SAR quantizer, an additional 1st-order noise shaping can be realized by the noise coupling technique. The proposed noise coupling technique is not requite using the active analog component, the lower consumption can be maintained. Furthermore, only two non-overlapped clocks are required for the proposed $\Delta\Sigma$AD modulator, which is realized by a sample clock generator. The $\Delta\Sigma$AD modulator circuit is realized by dynamic analog component, therefore the power consumption can be kept at a low level. The simulation results including both thermal noise and flicker noise show the feasibility of the proposed $\Delta\Sigma$AD modulator. This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

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