A 2nd-Order ΔΣAD Modulator Using Dynamic Analog Components with Simplified Operation Phase

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SUMMARY   A 2nd-order ΔΣAD modulator architecture is proposed to simplify the operation phase using ring amplifier and SAR quantizer. The proposed modulator architecture can guarantee the reset time for ring amplifier and relax the speed requirement on asynchronous SAR quantizer. The SPICE simulation results demonstrate the feasibility of the proposed 2nd-order ΔΣAD modulator in 90 nm CMOS technology. Simulated SNDR of 95.70 dB is achieved while a sinusoid −1 dBFS input is sampled at 60 MS/s for the bandwidth is BW=470 kHz. The power consumption of the analog part in the modulator is 1.67 mW while the supply voltage is 1.2 V.

key words: *ΔΣ modulator, ring amplifier, switched-capacitor circuit, successive-approximation-register ADC (SAR ADC)*

1. Introduction

High SNDR ADCs are widely used in the mixed-signal SoC in the fields of the both consumer and industrial applications. SAR ADCs are well known as an energy efficiency architecture for low and medium-speed, medium-resolution applications [1], [2]. Because the resolution of SAR ADC depends on the accuracy of capacitor matching and the offset of comparator, it is difficult to realize a high resolution SAR ADC in nanoscale CMOS technology. On the other hand, the ΔΣAD modulator reduces the quantization noise in the desired signal band by oversampling and noise-shaping technique, so that it is suitable to realize the high SNDR ADC in nanometer CMOS technology [3]. Normally, high SNDR modulator is realized by the techniques of high-order noise-shaping and/or higher oversampling ratio (OSR). However, high OSR needs high speed operation and increases the total power consumption of the modulator. High-order noise-shaping needs high order integrators with power hungry amplifier. Moreover, it is difficult to realize a high gain, low distortion, wide band-width amplifier in nanometer CMOS technology.

The feed-forward structure is a preferred architecture for ΔΣAD modulator to tolerate the distortion of the internal amplifier [4]. Multi-bit quantizer can also be chosen to relax the slew-rate requirement on the amplifier to reduce the power of the modulator [3]. When the multi-bit quantizer in the modulator is realized by a flash ADC, the power of the quantizer is still large because of the static current though

the resistance ladder and dynamic current of numerous comparators. Furthermore, in conventional feed-forward modulator, an active analog adder using an amplifier is necessary at the input node of the quantizer, which increase the power of the modulator.

In order to achieve the maximum power-efficiency of the amplifier in ADC, the use of the dynamic amplifier (eg. logic inverter or ring amplifier) instead of OTA has been proposed and results in dynamic-analog-components-based ADC [5], [6]. However, since the dynamic analog component needs the reset operation, it limits the operation speed of the circuit. In the previous work, we have proposed an implementation architecture of multi-bit feed-forward ΔΣAD modulator with passive analog adder and dynamic amplifier [7]. Simulation results also show the feasibility of ΔΣAD modulator with passive adder embedded SAR quantizer and ring amplifier. As mentioned above, the reset operation of the ring amplifier is required. Furthermore, an asynchronous SAR quantizer is used in the ΔΣAD modulator. To ensure the amplifier's reset time and asynchronous SAR ADC's operating time in the ΔΣAD modulator, 4 operation modes (4-phases) are required. As a result, the ΔΣAD modulator is complicated and the speed of operation is limited.

In this work, we propose a 3-phases ΔΣAD modulator with ring amplifier and passive adder embedded SAR quantizer to simplify the ΔΣAD modulator operation modes. The proposed ΔΣAD modulator can guarantee the reset time for ring amplifier and relax the speed requirement on asynchronous SAR quantizer. SPICE simulations have been done to verify the effectiveness of the proposed architecture and to confirm the performance of the modulator. The peak SNDR of 95.70 dB is reached while OSR=64 for sinusoid input at 219.7 kHz with −4.03 dBFS input amplitude.

2. Proposed ΔΣAD Modulator Architecture

Figure 1 shows the block diagram of 2nd-order ΔΣAD modulator using SAR ADC and ring amplifier in our previous work [7]. The switched-capacitor integrator of the ΔΣAD modulator is realized by the ring amplifier. The operation of ring amplifier is different from the conventional amplifier, the ring amplifier needs to operate alternately between the reset mode and the amplification mode. The output of ring amplifier is disabled at the reset mode, therefore, the load capacitance of the integrator must be connected to the output of the ring amplifier at the amplification mode. Furthermore, because SAR ADC is used as an internal quan-
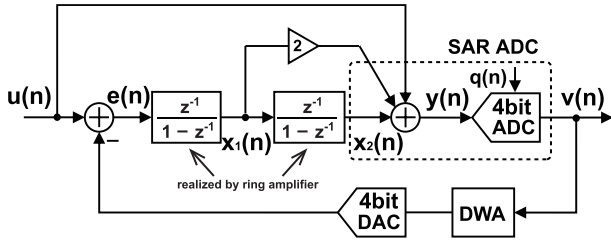
Fig. 1 A 2nd-order ΔΣAD modulator with SAR ADC [7].

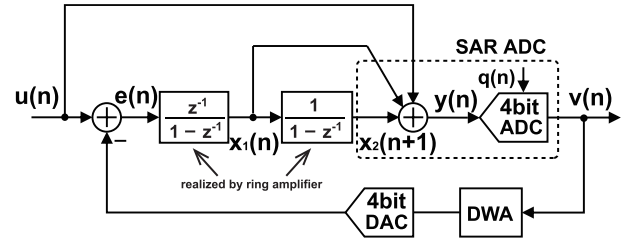**Fig. 2** Proposed architecture of the 2nd-order ΔΣAD modulator.

tizer in the ΔΣAD modulator, unlike the flash ADC, SAR ADC need to use an extra phase for the sampling operation. Due to the constraint of the above two factors, the clock timing design of the ΔΣAD modulator using ring amplifier and SAR ADC is much more difficult than the ΔΣAD modulator using the traditional amplifier and flash ADC. Therefore, the following four factors need to be guaranteed when designing the ΔΣAD modulator using ring amplifier and SAR ADC, 1 the sampling capacitor of the 2nd integrator and one of the sampling capacitors of the SAR ADC are connected to the output of the 1st integrator at the same time; 2) the sampling capacitor of the 1st integrator and one of the sampling capacitors of the SAR ADC are connected to input signal at the same time; 3) the successive approximation operation of asynchronous SAR ADC also need to use an extra phase; 4) the DAC embedded in the 1st integrator is driven by the output of the SAR ADC quantizer, therefore, the amplification operation of the 1st integrator need to wait for the feedback signal from the SAR ADC output.

Considering the above factors, in order to correctly implement the transfer function of the 2nd-order ΔΣAD modulator, the ΔΣAD modulator needs to be operated in 4-phases as shown in Fig. 3. Figure 3(a) shows the simplified circuit schematic diagram of the ΔΣAD modulator using SAR ADC and ring amplifier(R-AMP) in the previous work, its timing diagram and the operation mode diagram are shown in Fig. 3(b) and Fig. 3(c), respectively. The ΔΣAD modulator is complicated and the speed of operation is limited.

In this work, in order to simplify the operation phase of the ΔΣAD modulator to improve the speed of the ΔΣAD modulator, we propose the ΔΣAD modulator architecture as shown in Fig. 2 that allows the ΔΣAD modulator to work in 3-phases. Fig. 4(a) shows the simplified circuit schematic diagram of proposed ΔΣAD modulator using SAR ADC and ring amplifier(R-AMP) with the simplified operation phase in this work, its timing diagram and the operation mode diagram are shown in Fig. 4(b) and Fig. 4(c), respectively. The operation of the proposed modulator can be completed in 3-phases, so that the speed of modulator can be improved than that in the previous work. Although the operation timing of these two kinds of ΔΣAD modulator (Fig. 1 and Fig. 2) are different, the architecture of the proposed ΔΣAD modulator (Fig. 2) can still realize the 2nd-order noise shaping transfer characteristic that can be proved as the following.

In Fig. 2, u(n) is the input, v(n) is the output of the ΔΣAD modulator. The input signal of the quantizer y(n)

is given as

$$y(n) = u(n) + 2x_1(n) + x_2(n) \tag{1}$$

where $x_1(n)$ is the output signal of the 1st integrator, $x_2(n)$ is the output signal of the 2nd integrator.

Since the output signal of the 2nd integrator obeys the following relationship

$$x_2(n+1) = x_1(n) + x_2(n) \tag{2}$$

by combining it with (1) and (2) will lead to

$$y(n) = u(n) + x_1(n) + x_2(n+1) \tag{3}$$

Consequently, the architecture of the ΔΣAD modulator can be changed as shown in Fig. 2. The output signal of the ΔΣAD modulator is obtained as

$$v(n) = u(n) + q(n) + x_1(n) + x_2(n+1) \tag{4}$$

The z-domain expression of Eq. (4) can be expressed as

$$V(z) = U(z) + Q(z) + X_1(z) + X_2(z)z \tag{5}$$

In Fig. 2, the z-domain expression of the 1st and the 2nd integrator's outputs are given as

$$X_1(z) = [U(z) - V(z)]\frac{z^{-1}}{1 - z^{-1}} \tag{6}$$

$$X_2(z)z = \frac{X_1(z)}{1 - z^{-1}} \tag{7}$$

Substituting Eq. (6) and (7) into Eq. (5), we get

$$V(z) = U(z) + (1 - z^{-1})^2 Q(z) \tag{8}$$

The transfer function of the proposed ΔΣAD modulator expressed in Eq. (8) shows the 2nd-order noise shaping characteristic. It is the same as that in Fig. 1. The equivalence of the two kinds of ΔΣAD modulator architecture (Fig. 1 and Fig. 2) are confirmed. However, only 3 operation modes are required in the proposed ΔΣAD modulator, so that the operation speed of modulator can be improved.

3. Proposed ΔΣAD Modulator Implementation

Figure 5(a) illustrates the schematic diagram of the proposed ΔΣAD modulator using SAR ADC and ring amplifier(R-AMP) with the simplified operation phase in this work, its
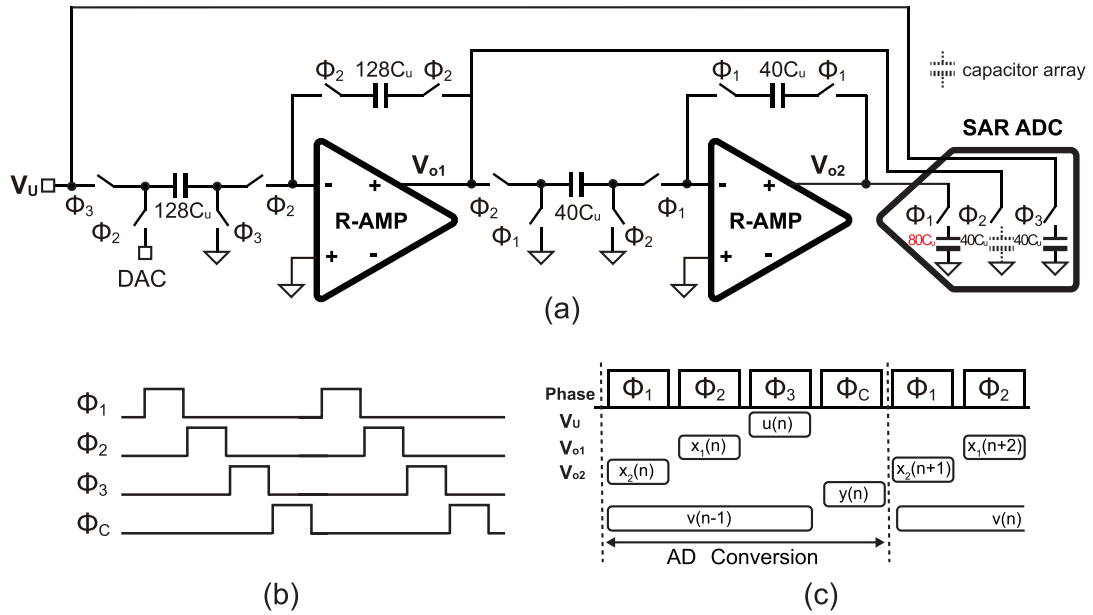
Fig. 3 Simplified circuit implementation of the proposed ΔΣAD modulator using SAR ADC and ring amplifier(R-AMP) in the previous work. (a)Simplified circuit schematic diagram. (b)Timing diagram. (c)Operation mode diagram.
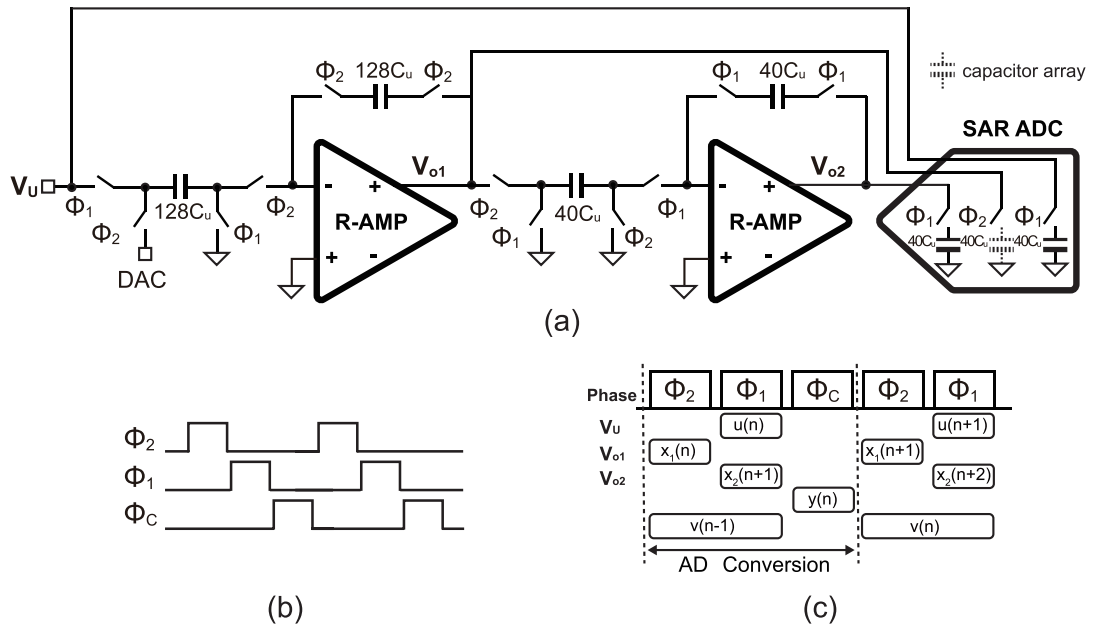

Fig. 4 Simplified circuit implementation of the proposed ΔΣAD modulator using SAR ADC and ring amplifier(R-AMP) with the simplified operation phase in this work. (a)Simplified circuit schematic diagram. (b)Timing diagram. (c)Operation mode diagram.

timing diagram is shown in Fig. 5(b). In the feed-forward ΔΣAD modulator, the input signal to the loop filter contains only the shaped quantization noise, so that the modulator can reduce the influence of amplifier's non-linearity for higher SNDR [4].

Moreover, the ring amplifier can realize higher gain than traditional amplifier at low supply voltage, and the static current of the ring amplifier is very small, so that the

power consumption of the modulator can be maintained low. An asynchronous SAR ADC is used as a 4-bit quantizer. It not only improve the stability of the modulator, but also relax the requirement on the slew-rate of amplifier. The 4-bit SAR ADC have 3 inputs terminal (V_U, V_{o1} and V_{o2}), since the SAR ADC converts the summation of them to digital code, the analog adder is realized by capacitor array without amplifier. Although the mismatches among the unit
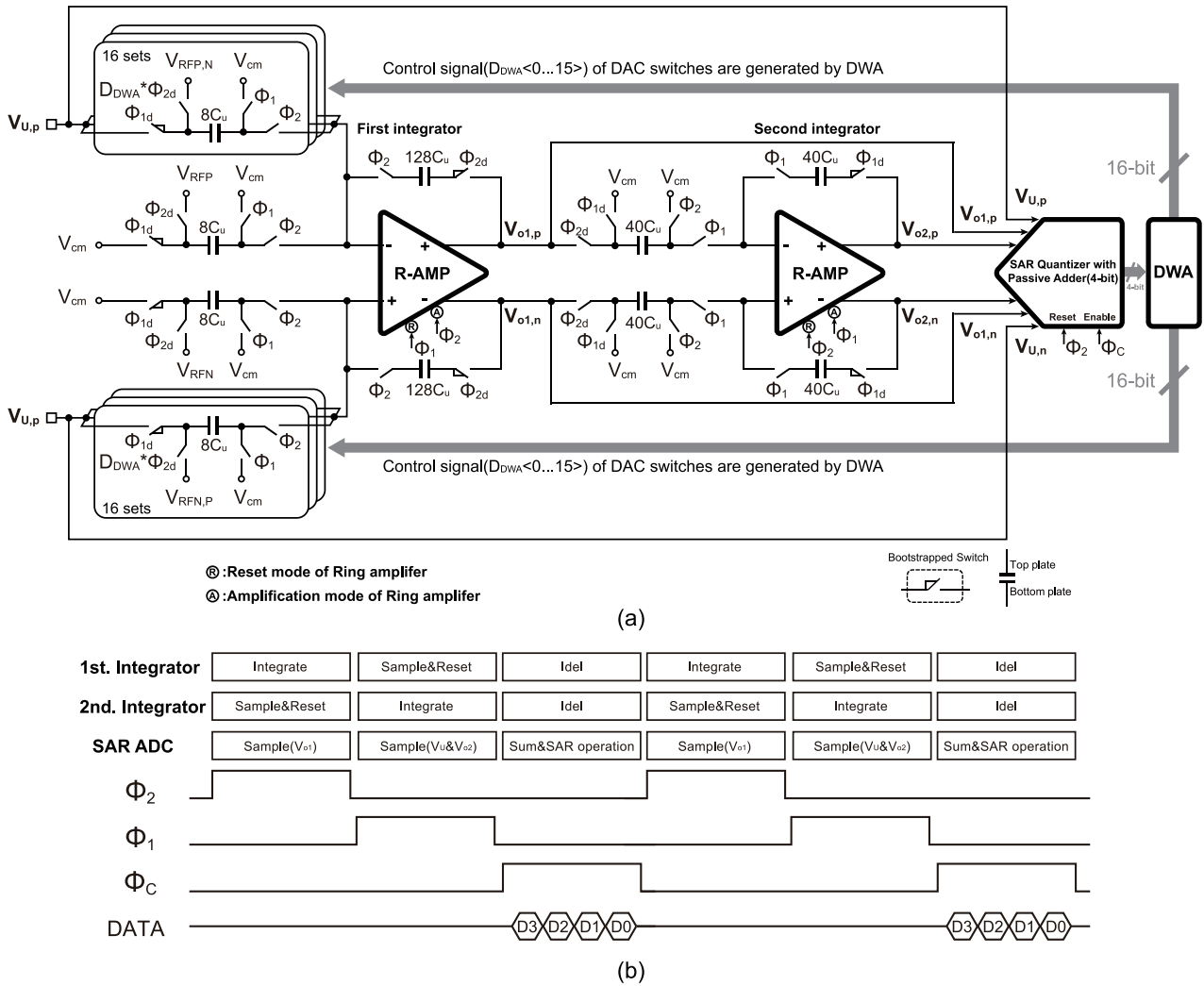
Fig. 5 Circuit implementation of the proposed ΔΣAD modulator using SAR ADC and ring amplifier(R-AMP) with simplified operation phase in this work. (a)Circuit schematic diagram. (b)Timing diagram.

elements in a multi-bit digital-to-analog convertor (DAC) cause the harmonic distortion in the signal band, the data-weighted-averaging (DWA) logic circuit is applied to the ΔΣAD modulator to reduce the influence of DAC nonlinearity errors [3].

3.1 Asynchronous SAR ADC with Passive Adder

Figure 6(a) shows the schematic diagram of the proposed charge redistribution asynchronous SAR ADC with passive adder. It consist of capacitor array, a dynamic comparator and asynchronous SAR logic circuits. Capacitors connected to V_U, V_{o2}, V_{o1} are used for a passive-adder, and the capacitors surround by the dash line are also used as the capacitor DAC for SAR DAC.

Figure 7 shows two operation modes for equivalent circuit of passive-adder. In the sampling mode, the bottom plate of sampling capacitors are connected to input signals of V_U, V_{o1} and V_{o2}, the top plate of sampling capacitors are

connected to V_{cm} as shown in Fig. 7(a), respectively. The capacitor ratio for 3 input signals is 1:1:1, then the total charge stored on the capacitors Q_S can be expressed as:

$$Q_S = 40C_u \times V_U + 40C_u \times V_{o2} + 40C_u \times V_{o1} \qquad (9)$$

In the summation mode shown in Fig. 7(b), the bottom plate of sampling capacitors are connected to V_{cm}. The total capacitance between the input node of the comparator and V_{cm} is $120C_u$. The total charge Q_C of this summation mode on capacitors is

$$Q_C = 120C_u \times V_{IN(P,N)} \qquad (10)$$

According to charge conservation law, we have

$$Q_C = Q_S. \qquad (11)$$

Then, we get that

$$V_{IN(P,N)} = \frac{Q_S}{120C_u} = \frac{V_U + V_{o2} + V_{o1}}{3} \qquad (12)$$
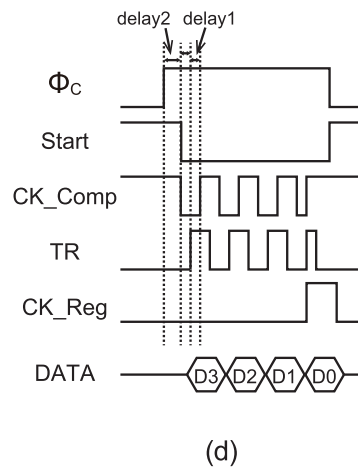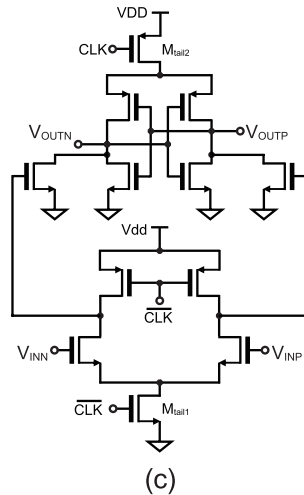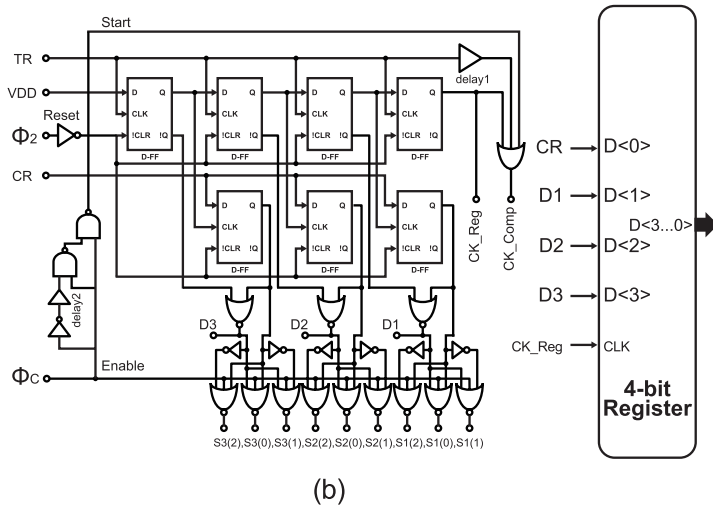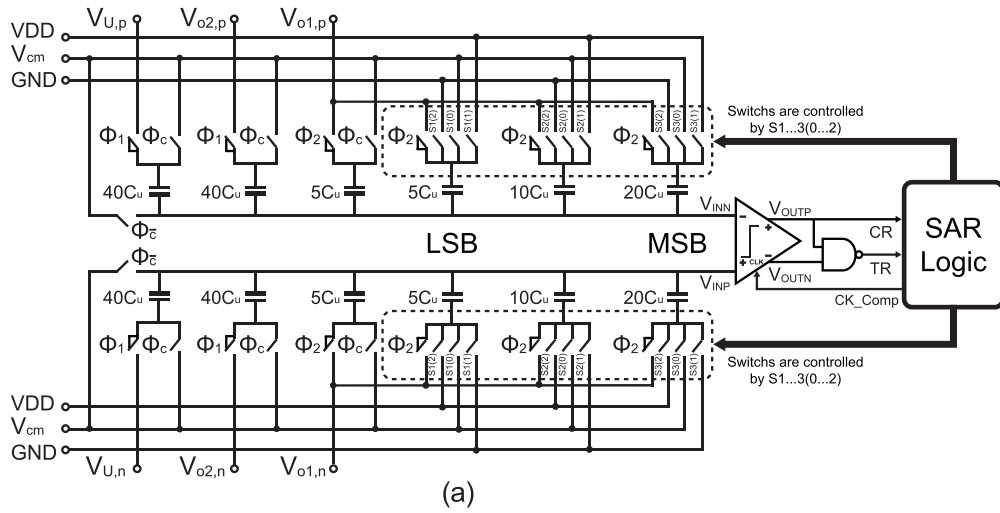
Fig. 6 Circuit implementation of the proposed charge redistribution asynchronous SAR ADC with passive adder. (a)Schematic diagram of the asynchronous SAR ADC with capacitor array passive adder. (b)Schematic diagram of asynchronous SAR logic. (c)Schematic diagram of the double-tail dynamic comparator used in SAR ADC. (d)Timing diagram of SAR logic circuit.
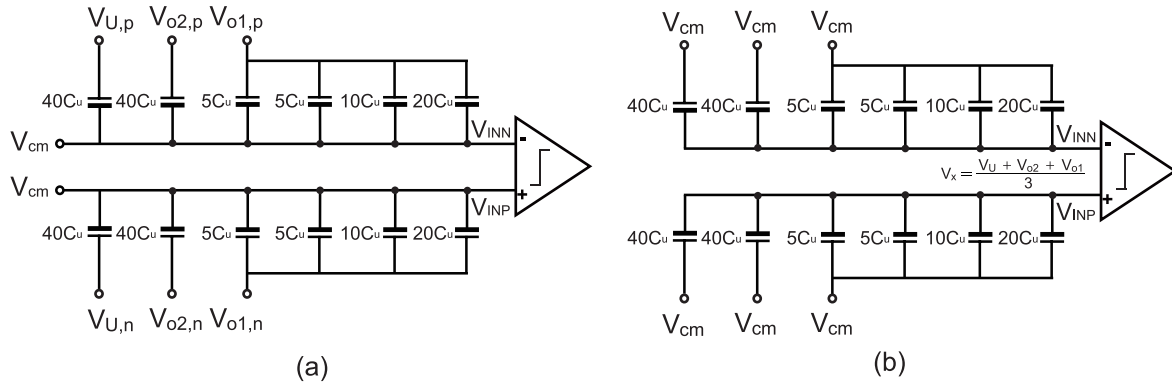
Fig. 7 Equivalent circuit of the proposed charge redistribution SAR ADC's operation. (a) Sampling mode. (b) Summation and successive approximation mode.

Equation (12) means that the summation of 3 input signals can be realized by the proposed sampling technique for capacitor array. After the analog input summation is finished, the AD conversion is carried out from MSB to LSB in the successive approximation manner.

Asynchronous SAR logic circuit is shown in Fig. 6(b), it generates the control signal to drive the capacitor switches of DAC in the SAR ADC. Φ_C is enable signal and Φ_2 is reset signal for the asynchronous SAR logic circuit. S1(1) and S1(2), S2(1) and S2(2), S3(1) and S3(2) are control signals for the DAC capacitor switches, which are connected to reference voltages, VDD and GND. S1(0), S2(0) and S3(0) are control signals for the DAC capacitor switches, which are connected to common voltage, V_{cm}. Fig. 6(c) shows the schematic diagram of the double-tail dynamic comparator used in SAR ADC [9]. This topology has less stacking current and therefore it can operate at lower supply voltages. The differential output nodes of the dynamic comparator are followed by a NAND gate as shown in Fig. 6(a). The inputs of NAND sense the toggle of differential comparator's output to realize the asynchronous operation of the SAR ADC. While the clock signal "CLK" of the comparator is High (M_{tail1} and M_{tail2} are off), the output nodes of comparator V_{OUTP} and V_{OUTN} are reset to VDD. While the clock signal "CLK" of the comparator changes from High to Low (M_{tail1} and M_{tail2} are turned on), the voltage comparison of two input nodes of V_{INP} and V_{INN} is done, the comparison result appears at nodes of V_{OUTP} and V_{OUTN}. The comparison result(signal "CR") is saved in the DFF(D Flip-flop) of the asynchronous SAR logic circuit provisionally, then the comparator changes to the latch mode. Because these two output nodes are bounded to the inputs of NAND gate, while the voltage comparison is finished, NAND gate outputs a trigger signal "TR" to drive the operation of the asynchronous SAR logic circuit. The buffer "delay1" inserted between the clock signal "TR" and one of the inputs of the 3-input OR gate that can prolong the usable DAC setting time, when the SAR ADC operates at the successive approximation mode. When the comparator makes the decision of the last bit(D0), the signal "CK_Reg" goes high to trigger the 4-bit register, the comparison results D3, D2, D1 (saved in the DFF pre-

viously) and the LSB result D0 (the last signal "CR") are transferred to 4-bit register as shown in Fig. 6(b). The buffer "delay2" is used for delaying the signal "Start" (enable signal of asynchronous SAR logic) that can prolong the setting time of passive adder, to guarantee the the addition result is complete settled (the charge redistribution on capacitor array to be finished) before AD conversion. Figure 6(d) shows the timing diagram of asynchronous SAR logic circuit. In a conventional synchronous SAR ADC, the speed of the comparator clock signal is limited by the worst-case cycle time. However, in the asynchronous SAR ADC, the signal "TR" is generated by NAND gate, so that the conversion steps are executed consecutively. Therefore, the speed of the asynchronous SAR logic is faster than that of the conventional synchronization SAR logic.

As mentioned above, the proposed SAR ADC realizes not only a 4-bit quantizer but also an analog adder with the capacitor array using a comparator, so that the power consumption of modulator can be reduce from the conventional feed-forward modulator using the active adder realized by amplifier. Furthermore, since SAR ADC is implemented by dynamic comparators and asynchronous successive approximation logic circuits [8], it can work at high speed.

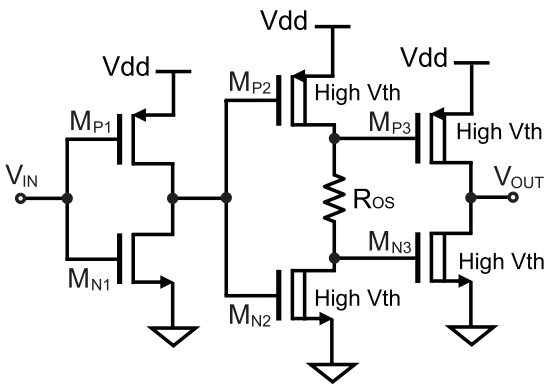### 3.2 Full Differential Ring Amplifier

The amplifier is the key components of the modulator to realize the integrator, and it is the most power-hungry circuit block in the modulator. Ring amplifier for multiplying digital-to-analog converter (MDAC) circuit has been proposed and demonstrated to reduce the power of the pipeline ADC [6], [10]. In this work, we use the full differential ring amplifier to reduce the power consumption and to extend the dynamic range of the $\Delta\Sigma$AD modulator at the same time.

Figure 8(a) shows the full differential ring amplifier with switched-capacitor common mode feedback (CMFB) structure. C_Cs are added to the input nodes of amplifier to realize the amplifier input offset cancellation for the integrator [6]. Figure 8(b) shows the schematic of the ring amplifier's core in the proposed $\Delta\Sigma$AD modulator with self bias circuit. It is constructed with cascaded 3-stage inverters, so that it
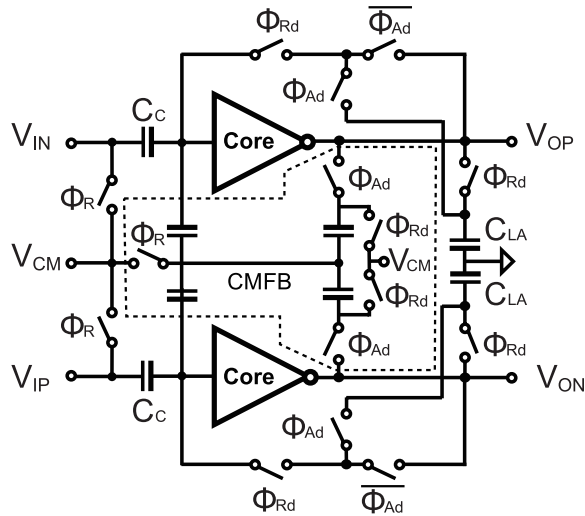
Φ_R :Reset mode of R-AMP
Φ_A :Amplification mode of R-AMP

(a)

(b)

Fig. 8 Schematic diagram of full differential R-AMP (a) R-AMP(Ring-Amplifier). (b) Core of R-AMP.

is similar to a ring oscillator in the amplifier. The input of the MOSFET M_{P1} and M_{N1} is biased at V_{cm} when the ring amplifier forms a feedback loop. Therefore, the M_{P1} and M_{N1} operate in the wake inversion region current during the steady state of the amplifier with a very low static. The inverter which consist of M_{P1} and M_{N1} behaves as a class-AB amplifier providing high DC-gain and good linearity. Resistor R_{OS} is inserted to the output of the 2nd stage inverter. The R_{OS} not only compress the drain-source voltage of the M_{P2} and M_{N2} to the boundary between the weak and strong inversion regions for obtaining both high DC-gain and wide gain-bandwidth product [5], but also to generate the different offset voltages to the gate of the M_{P3} and M_{N3}. During the steady state, the gate-source voltage of the both M_{P3} and M_{N3} are set at less than their threshold voltage, thus the M_{P3} and M_{N3} are cut off, there is not static current flow thouth the

(a)
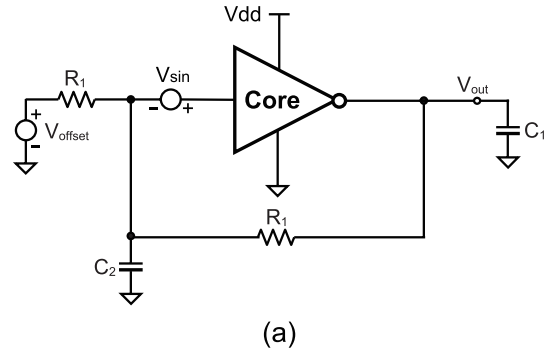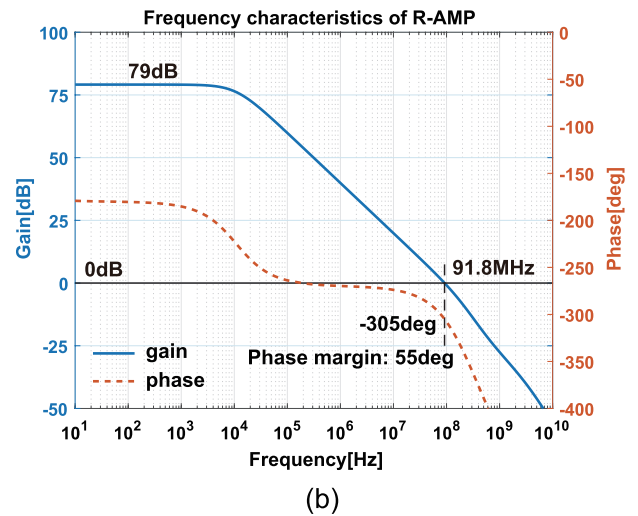
Fig. 9 AC analysis of R-AMP. (a) Simulation circuit. (b) Frequency characteristics of R-AMP.

amplifier. During transition state, one of the two transistors M_{P3}, M_{N3} is operating in the strong inversion region, while the other one is set to off state completely, so that higher slew rate can be realized. The push-pull inverter which consist of M_{P3} and M_{N3} behaves as a class-C amplifier and the rail-to-rail output is allowed for the ring amplifier. The setting time and power consumption of the ring amplifier can be reduced dramatically. Moreover, high threshold voltage $M_{P2,3}$ and $M_{N2,3}$ are used in the 2nd and 3rd-stage to extend the stable offset voltage range for the amplifier.

In order to confirm the performance of ring amplifier, SPICE simulation of AC analysis is introduced using the circuit shown in Fig. 9(a). The SPICE simulation result is shown in Fig. 9(b). The DC gain of ring amplifier reached to 79dB with 55° phase margin and 91.8MHz unity-gain bandwidth. Simulation parameters of the ring amplifier are shown in Table 1.

3.3 Multi-Bit DAC and DWA Logic Circuit

A 4-bit capacitor DAC is used for the 1st integrator as shown in Fig. 5, the mismatches among the unit elements in a multi-bit DAC cause the harmonic distortion in the signal band, the data-weighted-averaging (DWA) logic circuit [11] is applied to the ΔΣAD modulator to reduce the influence of
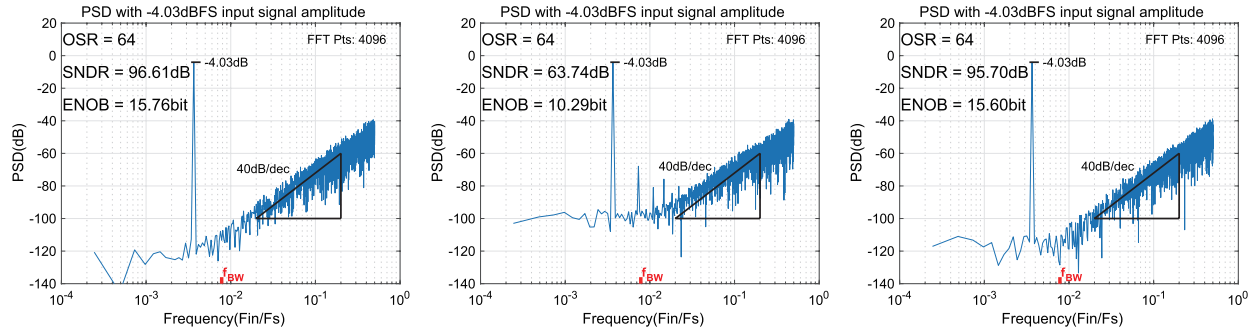
Fig. 10 SPICE simulated results comparison of $\Delta\Sigma$AD modulator power spectrum with different DACs. (a) An ideal DAC. (b) DAC with 1% unit capacitance mismatches at DWA OFF Mode. (c) DAC with 1% unit capacitance mismatches at DWA ON Mode.

Table 1 Simulation parameters of R-AMP.

Technology	TSMC 90 nm CMOS
Supply voltage	1.2 V
V_{offset}	0.6 V
R_1	10 GΩ
C_1	640 fF
C_2	1 uF

Table 2 Simulation parameters of $\Delta\Sigma$AD modulator.

Technology	TSMC 90 nm CMOS
Supply voltage	1.2 V
Input frequency	219.7 kHz
Input amplitude	2 Vpp
Sampling rate	60 MS/s

Table 3 Performance summary and comparison with previous works.

Specification	Chao[13]	Chao[8]	Pan[12]	This work
Technology(nm)	90	90	90	90
Supply voltage(V)	1.2	1.2	1.2	1.2
Sampling rate (MS/s)	80	60	50	60
OSR	16	16	64	64
Signal BW (MHz)	2.5	1.875	0.39	0.47
SNDR (dB)	81.97	78.8	80.84	95.7
Power (mW)	2.53	1.59	1.88	1.67
FOMS (dB)	169.7	168.0	161.5	180.2

DAC nonlinearity errors. To illustrate the effect of the DWA logic circuit, SPICE simulation comparison with the proposed modulator is performed in 3 cases: (1) an ideal 4-bit DAC without any capacitance variation; (2) 4-bit DAC with 1% unit-capacitance mismatches while DWA at OFF mode; (3) 4-bit DAC with 1% unit-capacitance mismatches while DWA at ON mode. The output spectrum for the above 3 cases are shown in Fig. 10(a), (b) and (c), respectively. In the ideal case shown in Fig. 10(a), the quantization noise is shaped out from the signal band. While the unit-capacitance of DAC is variated without DWA, the non-linearities of DAC raise the in-band noise floor, and cause the harmonic distortion as shown in Fig. 10(b). On the other hand, while DWA technique is applied, not only the in-band noise but also the harmonic distortion in the signal band are noise-shaped as shown in Fig. 10(c).

4. Simulation Results of the Proposed $\Delta\Sigma$AD Modulator

The propose $\Delta\Sigma$AD modulator shown in Fig. 5 is designed in TSMC 90 nm CMOS technology. The switched-capacitor integrators are realized by ring amplifier. The quantizer is a 4-bit SAR ADC with the embedded passive adder. 4-bit DAC on the feedback path is constructed by capacitor array. The DWA logic circuit is designed to reduce the influence of the nonlinearities which occurred by the capacitors mismatch of the multi-bit DAC [3]. SPICE simulations have been done to confirm the performance of the modulator and to verify the effectiveness of the proposed architecture. The simulation parameters are shown in Table 2. Figure 10(c)

shows the simulated spectrum result of the proposed modulator with 1% DAC unit-capacitance mismatches.

The peak SNDR of 95.70 dB is reached while OSR = 64 for a sinusoid input at 219.7 kHz with −4.03 dBFS input amplitude (The thermal noise of the modulator is not included in the SPICE simulation). The power consumption of analog part in the proposed modulator is 1.67 mW at 1.2 V supply. The performance of the proposed $\Delta\Sigma$AD modulator is summarized in Table 3 in comparison with the previous works. Although the signal band of our proposed $\Delta\Sigma$AD modulator is less than other works, the operation speed and power consumption are comparable to other works. Needless to say, the SNDR and FoMS of the prototype modulator should be degraded from the SPICE simulation results. However, the operation speed and the power consumption often meet the comparable value to simulation results.

5. Conclusions

A 2nd-order ΔΣAD modulator with the simplified operation phase using ring amplifier and SAR ADC has been designed in 90nm CMOS technology. Benefit from the reduction of the number of the ΔΣAD modulator operation phase, the speed of ΔΣAD modulator can be improved. Moreover, the ΔΣAD modulator is designed as the 2nd-order feed-forward architecture for reducing the influence of amplifier's non-linearity, and the SAR quantizer with passive-adder is used instead of quantizer and active adder. The ΔΣAD modulator circuit is realized by dynamic amplifier and a dynamic comparator, therefore the power consumption can be kept at a low level. Simulation results show the feasibility of the proposed ΔΣAD modulator.

Acknowledgments

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