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PAPER *Special Section on Analog Circuit Techniques and Related Topics*

A 12-bit 1.25 MS/s Area-Efficient Radix-Value Self-Estimated Non-Binary Cyclic ADC with Relaxed Requirements on Analog Components

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SUMMARY A 12-bit 1.25 MS/s cyclic analog-to-digital converter (ADC) is designed and fabricated in 90 nm CMOS technology, and only occupies an active area as small as 0.037 mm^2. The proposed ADC is composed of a non-binary AD convertion stage, and a on-chip non-binary-to-binary digital block includes a built-in radix-value self-estimation scheme. Therefore, althouh a non-binary convertion architechture is adopted, the proposed ADC is the same as other stand-alone binary ADCs. The redundancy of non-binary 1-bit/step architecture relaxes the accuracy requirement on analog components of ADC. As a result, the implementation of analog circuits such as amplifier and comparator becomes simple, and high-density Metal-Oxide-Metal (MOM) capacitors can be used to achieve a small chip area. Furthermore, the novel radix-value self-estimation technique can be realized by only simple logic circuits without any extra analog input, so that the total active area of ADC is dramatically reduced. The prototype ADC achieves a measured peak signal-to-noise-and-distortion-ratio (SNDR) of 62.3 dB using a poor DC gain amplifier as low as 45 dB and MOM capacitors without any careful layout techniques to improve the capacitor matching. The proposed ADC dissipated 490 μW in analog circuits at 1.4 V power supply and 1.25 Msps (20 MHz clocking). The measured DNL is +0.94/ − 0.71 LSB and INL is +1.9/ − 1.2 LSB at 30 kHz sinusoidal input.

key words: *cyclic ADC, non-binary ADC, radix-value estimation algorithm, β-expansion, multiply-by-β MDAC.*

1. Introduction

SAR ADCs have been recommended as the most power-efficient architecture for the low-voltage energy-hungry applications [1]. However, the input capacitors in high-resolution SAR ADCs require large size to satisfy the mismatch requirement. Since some additional high driving capability circuits should be provided to charge the large capacitors, the SAR ADCs might lead to more power consumption. Moreover, in the cases of applications which require multiple channel ADCs integrated in a single chip, the area efficiency would be a much more important concern [2]. Because the large capacitors need more silicon areas, the active area of high-resolution SAR ADC becomes significantly larger than other ADC architectures. To resolve the design issues as described above, this paper presents an area-efficieny cyclic ADC which integrates a compact analog part for non-binary A-to-D conversion and a simple digital part for non-binary to binary encoding with self-estimated radix-value [3]. In our previous work, we have proposed an analog to non-binary digital converter structure with radix-value estimation algorithm, and demonstrated the analog area efficiency of non-binary architecture [4], [5]. In this work, we propose the implementation circuit for radix-value self-estimation and binary-to-non-binary encoding with simple logic circuits and a loo-up-table (LUT). We also give the details and design consideration points for the implementation of LUT. As a result, the proposed ADC can work as a standalone binary ADC although an internal non-binary architecture is provided.

The redundancy of non-binary ADC tolerates the non-linear conversion errors caused by the offsets of comparator and/or amplifier, so that a simple 1-bit (not 1.5-bit or multi-bit) multiplying digital-to-analog converter (MDAC) architecture can be used for the analog part of the proposed ADC. It consists of only one comparator, one amplifier and small area capacitors. A 1.5bit MDAC conversion stage architecture for binary ADC can also tolerate the offsets of comparator and/or amplifier [6], however, well matched capacitor ratio and high gain amplifier are necessary to realize required linearity for a high resolution ADC. On the other hand, in a non-binary ADC, because the nonlinear errors which come from the mismatches of capacitors and finite DC gain of amplifier are totally corrected by the proposed on-chip radix-value self-estimation scheme in the digital domain, circuit design consideration only put on the thermal noise requirement, regardless of the capacitors mismatch and the finite gain of amplifier. Therefore, the analog part is realized in a small area by using high-density MOM capacitors and a compact poor gain amplifier without any careful layout techniques to improve the matching. Although some digital calibration techniques have been so far reported to relax the accuracy requirements on the analog elements in ADCs [1], [7], the algorithms and their realization circuits are still complex and the extra analog input is required, so that calibration time is too long to be used effectively. On the other hand, our proposed radix-value self-estimation scheme is realized efficiently by simple digital circuits without any extra analog input. Consequently, not only the analog area but

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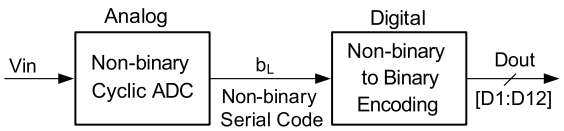

Fig. 1 Block diagram of the proposed cyclic ADC.

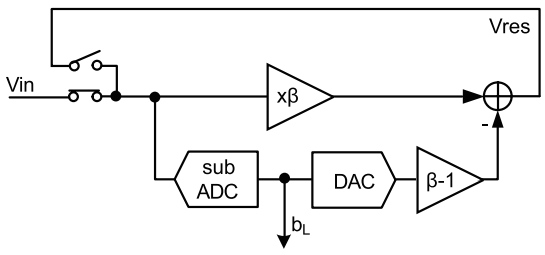

Fig. 2 Simplified analog part of the non-binary cyclic ADC.

also the digital area of ADC can be reduced effectually. We achieved the most area-efficient prototype ADC compared to so far reported ADCs with similar resolutions.

2. Proposed Cyclic ADC Architecture

Figure 1 shows a block diagram of the proposed cyclic ADC. It consists of an analog part as a front-end and a digital part as a back-end. The analog part converts the analog input signal V_{in} to digital codes b_L with a non-binary radix. The digital part covers the radix-value self-estimation and non-binary to binary encoding.

2.1 Front-End Analog Circuit Structure

In order to minimize the analog area, a simple 1-bit structure is chosen for the front-end A-to-D conversion stage. As shown in Fig. 2, the analog part contains a 1-bit sub-ADC (comparator), a 1-bit DAC, an analog subtractor, and a multiply-by-radix (radix=β, $1<\beta<2$) amplifier. This conversion stage is similar to a conventional binary structure with MDAC [6]; however, a multiply-by-β amplifier is used instead of a multiply-by-2 amplifier; simultaneously, the DAC output is scaled by β-1. This stage resolves one bit per conversion and feeds back the residual signal to the input node for the next conversion step. The residue is converted incrementally to perform a high-resolution conversion.

Figure 3 shows the simplified switched-capacitor configuration of this conversion stage in a single-end scheme (the actual design is a fully differential structure); and Fig. 4 illustrates the operation of the multiply-by-β amplifier. During the sampling phase shown in Fig. 4(a), the analog input V_{in} is sampled by the capacitors C_s and C_f. During the amplifying phase shown in Fig. 4(b), C_f is connected to the output of the amplifier V_{res}, and C_s is connected to the reference voltage of $+V_{ref}$ or $-V_{ref}$, depending on the output code of sub-ADC b_L. Assuming that the amplifier DC gain is $A_0=\infty$, while $(C_s+C_f)/C_f=\beta$, the residue is expressed as

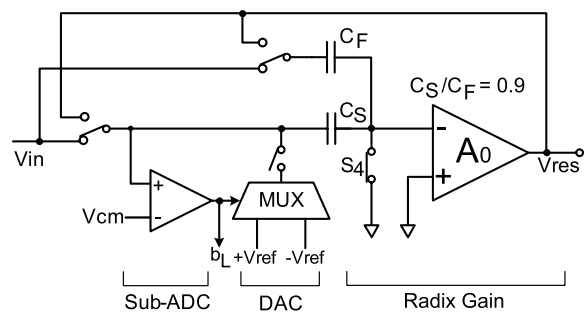

Fig. 3 Switched-capacitor implementation of non-binary A-to-D conversion stage.

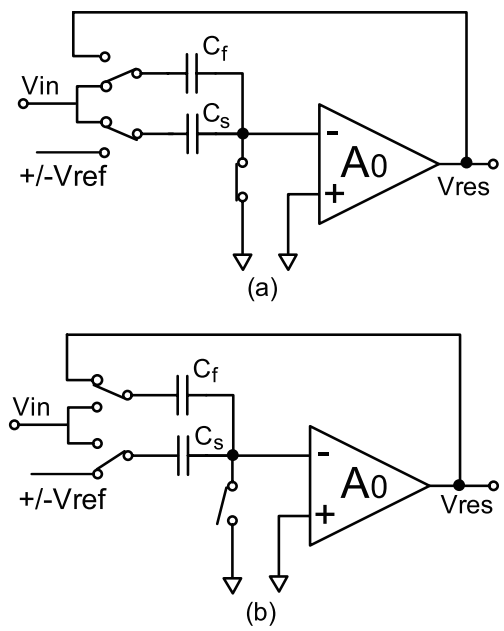

Fig. 4 Switched-capacitor multiply-by-β amplifier. (a) Sampling phase. (b) Amplifying phase.

$$V_{res} = \frac{C_s + C_f}{C_f} V_{in} \pm \frac{C_s}{C_f} V_{ref} = \beta V_{in} \pm (\beta - 1) V_{ref}. \quad (1)$$

When the amplifier DC gain A_0 is finite, the residue of the conversion stage is represented as

$$\begin{aligned} V_{res} &= \frac{A_0}{\beta + A_0}\left(\beta V_{in} \pm (\beta - 1) V_{ref}\right) \\ &= \beta_{eff} V_{in} \pm (\beta_{eff} - 1) h V_{ref}. \end{aligned} \quad (2)$$

Here, $\beta_{eff} = k\beta = k(C_s+C_f)/C_f$, $h = k(\beta\text{-}1)/(k\beta\text{-}1)$, and $k = A_0/(\beta+A_0)$. Figure 5 shows the transfer characteristic of the conversion stage. Since radix $\beta<2$, the redundancy of this non-binary conversion stage tolerates the offsets caused by comparator and amplifier. Equations (1) and (2) show that multiply-by-radix amplification can be realized only by changing the capacitors ratio of the conventional MDAC in binary ADC [6]. However, the mismatch of capacitors and degradation of amplifier DC gain cause random radix-value variation. In order to guarantee the linearity of the ADC, non-binary to binary encoding should be performed by using

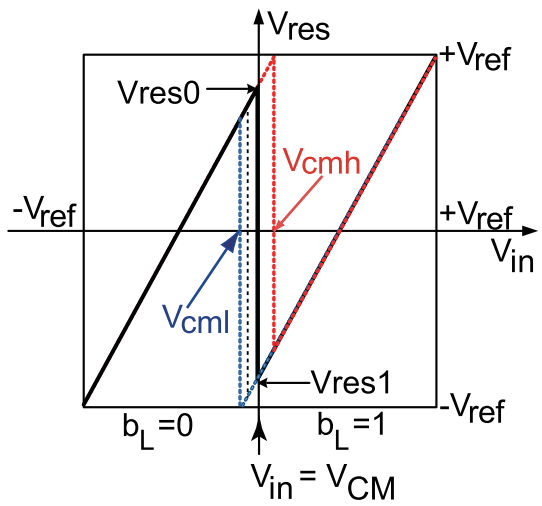

Fig. 5 Transfer characteristic of the non-binary conversion stage.

an exact effective radix-value of β_{eff}. As explained later, in this prototype non-binary ADC, neither accurately matched capacitor nor high-gain amplifier is required because the uncertain radix-value can be estimated by on-chip logic circuits. We just use this simple 1 bit multiply-by-radix structure to get the non-binary digital output code and amplify the residue for the next conversion step with the minimum analog circuits [5].

2.2 Back-End Digital Circuit Structure

The back-end digital part executes two main functions: one is the radix-value self-estimation, and the other is non-binary to binary encoding. In our implementation, the analog part outputs a 16-bit serial digital code b_L for each conversion. Then, b_L is converted to parallel 16-bit non-binary code B_L and 12-bit binary code D_N corresponding to the analog input as follows:

$$\frac{V_{in}}{V_{FS}} = (\beta - 1)\sum_{L=1}^{16}\frac{1}{\beta^L}B_L = \sum_{N=1}^{12}\frac{1}{2^N}D_N. \quad (3)$$

According to Eq. (3), two problems must be resolved to guarantee the linearity of this non-binary ADC. First, non-binary to binary encoding must be performed using an exact radix-value. However, the radix-value is uncertain due to the variation of circuit components, supply voltage and ambient temperature. Second, because the radix-value is not an integer, the complex multiplication and summation are required to obtain the actual binary code corresponding to the input signal. Therefore, the calculation circuits become complicated, and this factor leads to a more chip area and more power consumption. The proposed digital part shown in Fig. 6 consists of a serial-to-parallel circuit, a radix-value estimation block, a non-binary to binary conversion block and a read-only-memory (ROM) block. The ROM is filled with pre-calculated binary data, and used as a look-up table (LUT) for radix-value estimation and encoding. It is

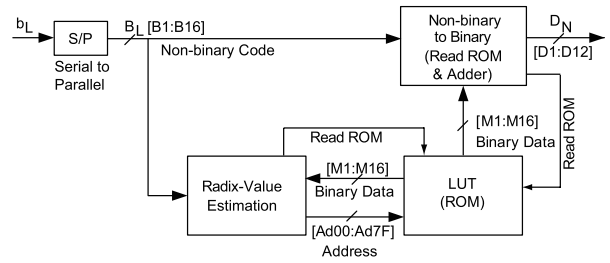

Fig. 6 Block diagram of digital part of the non-binary cyclic ADC.

Table 1 Binary data in ROM.

	Addr_r	00	01	···	0E	0F
Addr_c	Radix=β	(β-1)/β	(β-1)/β^2	···	(β-1)/β^{15}	(β-1)/β^{16}
00	1.7869	M[0000]	M[0001]	···	M[000E]	M[000F]
01	1.7878	M[0100]	M[0201]	···	M[010E]	M[010F]
02	1.7887	M[0200]	M[0201]	···	M[020E]	M[020F]
⋮	1.***	M[xx00]	M[xx01]	···	M[xx0E]	M[xx0F]
7E	1.8991	M[7E00]	M[7E01]	···	M[7E0E]	M[7E0E]
7F	1.9000	M[7F00]	M[7F01]	···	M[7F0E]	M[7E0F]

employed to simplify the calculation, and to minimize the digital area. As shown in Table 1, we calculated the binary data M[xxxx] as coefficients for $(\beta - 1)/\beta^L$ (L = 1, 2, 3, ..., 15, 16) with the different radix-value in advance and stored the calculation results into the ROM. By recalling the pre-calculated binary data corresponding to the non-binary code in the ROM, the encoding can be completed only by ROM and adder circuits without any multiplier. All calculations for the radix-value estimation and non-binary to binary conversion are carried out by using this LUT.

2.3 ROM Size Optimization

ROM occupies the dominant circuit area in the digital part. As shown in Table 1, since ROM size is proportional to the row numbers (bit numbers of non-binary code, L), the column numbers (radix-value variation steps, S) and the bit length of the stored binary data (bit numbers of M[xxxx], K), we must optimize the design parameters L, S and K to minimize the ROM area. Because the quantization error of L-bit non-binary ADC should be less than that of the required N-bit binary ADC, then we have

$$\frac{1}{(\beta - 1)\beta^L} < \frac{1}{2^N} \quad \Rightarrow \quad L > \frac{N - \log_2(\beta - 1)}{\log_2 \beta}. \quad (4)$$

While $1.5 \leq \beta < 2$, the minimum value of $\log_2(\beta - 1)$ is -1. For a 12-bit ADC, we get $L > (12+1)/\log_2 \beta$. In our implementation, the capacitor ratio is designed as $(C_s + C_f)/C_f = 1.9$, and the low DC gain amplifier with 45 dB is used, then the theoretical effective radix-value of 1.8799 is obtained by Eq. (2). Assuming the capacitor ratio mismatch is less than ±1%, and the variation of the finite amplifier DC gain is from 31 dB to 46 dB, the radix-value variation range from 1.7869 to 1.9000 is needed. Then, the non-binary bit number is given by $L > (12+1)/\log_2 1.7869 = 15.52$. Therefore,

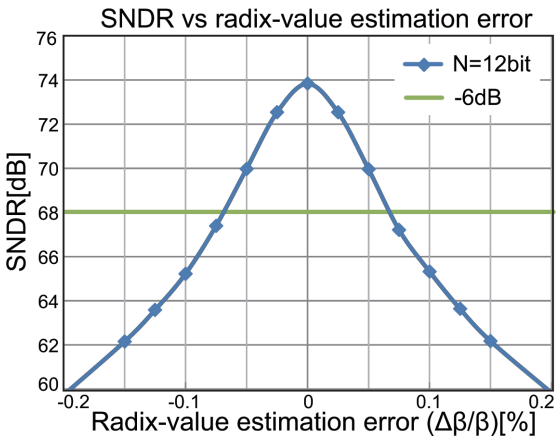

Fig. 7 ADC SNDR vs. radix-value estimation error.

L=16-bit non-binary code is used to satisfy the required resolution of 12-bit binary ADC. In order to determine the parameter K or the bit length of stored binary data in ROM, we consider the truncation error in the non-binary to binary encoding with a non-integer radix-value. This truncation error also should be less than the quantization error of binary ADC, then we have

$$\frac{L}{2^K} \leq \frac{1}{2^N} \quad \Rightarrow \quad K \geq N + \log_2 L. \tag{5}$$

While N=12 and L=16, we determine the bit length of binary data in ROM as K=16. In order to determine the radix-value variation steps S in ROM, we would consider the trade-offs of the ADC resolution, the radix-value estimation error and the chip area. High accurate radix-value variation steps are desired for high-resolution conversion. However, a high accurate radix-value leads to more ROM size and a large chip area. We made the MATLAB simulation to clarify the relationship between SNDR of binary ADC and the radix-value estimation error of non-binary code. Figure 7 shows the simulation results of SNDR against the radix-value estimation error for 12-bit binary ADC. In our simulation, variated radix-values are used for non-binary-to-binary encoding. SNDR values are calculated with binary output code of ADC. According to this simulation results, we recognized that the radix-value estimation error should be less than 0.05% to satisfy required accuracy for a 12 bit resolution ADC. In this implementation, the requirement for the radix-value error less than 0.05% is achieved by dividing radix-value variation range from 1.7869 to 1.9000 into S=128 steps which means that the column address (Addr_c) is represented by 7 bit. According to the above discussions, the total ROM size is determined as $16 \times 16 \times 128 = 32768$ bits.

2.4 Radix-Value Self-Estimation Circuits

The key point of the above non-binary to binary encoding is to use an exact radix-value. We proposed radix-value self-estimation circuits to obtain the effective radix-value simply with the utilization of redundancy in a non-binary ADC. As shown in Fig. 5, while we short the differential input nodes of the ADC (that means the input signal V_{in} is fixed to the analog common level of V_{CM}) and run A-to-D conversion, then we can obtain two digital codes as follows:

$$B_{Lm0} = [0, b_{02}, ..., b_{0N-1}, b_{0L}] \ (b_{01} = 0), \tag{6}$$
$$B_{Lm1} = [1, b_{12}, ..., b_{1N-1}, b_{1L}] \ (b_{11} = 1), \tag{7}$$

which correspond to the residue signals of V_{res0} and V_{res1} in Fig. 5, respectively. Here, B_{Lm0} and B_{Lm1} are obtained by holding MSB to 0 and 1, respectively. In a non-binary ADC, redundant digital codes B_{Lm0} and B_{Lm1} represent the same analog input despite the offset voltage of the comparator. Because ONE analog input of V_{in} can be expressed by TWO digital codes as

$$B_{Lm0} = B_{Lm1} = \sum_{l=1}^{L} \beta^{l-1} b_{0n} = \sum_{l=1}^{L} \beta^{l-1} b_{1l}, \tag{8}$$

then the solution of β in Eq. (8) gives the effective radix-value of the non-binary ADC. For example, V_{res0} and V_{res1} are converted to 5-bit digital codes as follows:

$$V_{res0}(Analog) \Leftrightarrow B_{Lm0}(Digital) = [0, 1, 1, 1, 0],$$
$$V_{res1}(Analog) \Leftrightarrow B_{Lm1}(Digital) = [1, 0, 0, 0, 1].$$

When B_{Lm0} and B_{Lm1} are substituted into Eq. (8), we obtain

$$B_{Lm0} = B_{Lm1} = \beta^3 + \beta^2 + \beta^1 = \beta^4 + \beta^0. \tag{9}$$

The solution of β in Eq. (9) is β=1.772. This result implies that an unknown value of β (as the same of the radix-value of the ADC) can be calculated from the above digital codes of B_{Lm0} and B_{Lm1}. To avoid complex calculation which resolves a high-order equation of β from Eq. (8), we proposed an efficient method using the difference between the two digital codes of B_{Lm0} and B_{Lm0}. The difference between the digital codes of B_{Lm0} and B_{Lm0} can be expressed as

$$e(\beta) = \sum_{n=1}^{N} \beta^{n-1} (b_{0n} - b_{1n}). \tag{10}$$

According to our simulation results, $e(\beta)$ is a monotone function of β in the range of $1.5<\beta<2$. Therefore, sweeping the β-value, the effective radix-value can be obtained when $|e(\beta)|$ is nearest to 0.

This radix-value estimation is realized easily by changing the column addresses of the ROM in the binary search manner to change the β-value. To avoid the radix-value estimation error caused by random noise, the radix-value is searched 32 times and averaged by on-chip circuits to guarantee the radix-value estimation error is less than 0.05% (as shown in Fig. 7) for 12-bit resolution ADC. Therefore, the nonlinear errors caused by capacitor mismatch and the finite gain of the amplifier can be entirely resolved while non-binary encoding is realized with the self-estimated effective radix-value. This foreground radix-value self-estimation

technique is effective to avoid the influences of the variation of the process, supply voltage, and temperature. As a result, the accuracy requirements on analog components of the proposed ADC can be greatly relaxed. When the differential input nodes of the ADC are shorted, the both nodes are connected to the analog common level in the estimation process. All of the above operations can be controlled by simple logic circuits, and the radix-value self-estimation can be carried out when we switch on this function. In our implementation, the digital part which includes ROM, clock generator, calculator and control logic are realized by only 7k gates (in terms on NAND gate).

3. Implementation and Experimental Results

The proposed cyclic ADC was designed and fabricated with TSMC 90nm CMOS technology without any option such as precision capacitors and low-threshold voltage transistors. Bootstrapped switches are used at the input of the ADC to reduce the nonlinear effect of ON-resistance [6], whereas all the others are CMOS switches. A latched comparator without any offset cancellation is used as the sub-ADC. A single-stage folded-cascode amplifier is used, and the simulated result of the DC gain is 45 dB while the analog supply voltage is 1.4 V. Since we aim to prove the validity of area-efficiency with the proposed architecture and radix-value self-estimation technique, we do not optimize the comparator and amplifier for the low power consumption.

The capacitors in the MDAC were chosen as C_s=270 fF and C_f=300 fF to satisfy the required thermal noise for 12-bit resolution. As a result, the nominal radix-value of non-binary ADC is approximately 1.90. Since the radix-value self-estimation technique tolerates radix-value variations caused by capacitor mismatch, the capacitor ratio of C_s/C_f is laid out only by the simple area ratio of two capacitors without unit-capacitor cell and dummy capacitors. High density MOM capacitors were used to reduced the chip area, and any special layout techniques are not employed to improve capacitor matching. The attention paid only to keeping the sensitive signals away from the noisy digital signal paths. Since the on-chip LUT is used for radix-value estimation and non-binary to binary encoding, different from the non-volatile memory used for complexible signal processing system, the ROM in our implementation is realized by the wired logic with single transistor switch. Radix-value estimation logic and ROM are synthesized with VHDL and implemented by automatic layout using standard cell. Figure 8 shows a microphotograph of the experimental prototype and the layout of the ADC. The active core size of the ADC is 0.037mm^2, which includes 114×58 μm^2 for the analog part and 207×145 μm^2 for the digital part.

Figure 9 shows the measured output power spectrum of the ADC. The peak SNDR is 62.25 dB while a sinusoid differential input of 30.2 kHz with 1.0 Vpp is sampled at 1.25 MS/s. The total power consumption of prototype ADC is 1.38 mW of which 0.49 mW for analog, 0.28 mW for digital and 0.61 mW for bias circuits. Figure 10 shows that the measured DNL is +0.94/−0.71 LSB, and INL is +1.9/−1.2 LSB. These experimental results show that our proposed architecture and radix-value self-estimation scheme make it easy to design high-resolution ADCs using the relaxed-accuracy analog components and simple logic circuits. The performance of the proposed ADC is summarized in Table 2 in comparison with the previous works. The proposed ADC occupies a small area as 0.037 mm^2, which is the smallest area compared with the similar resolution ADCs.

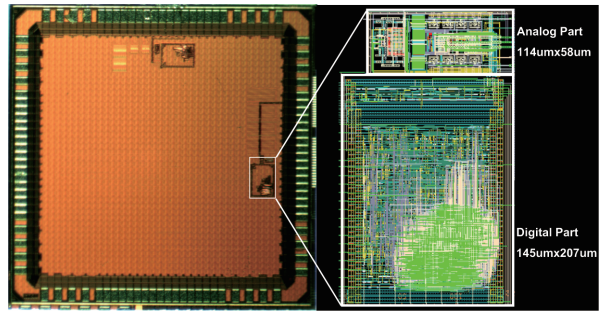

Fig. 8 Chip micrograph and layout of the prototype ADC.

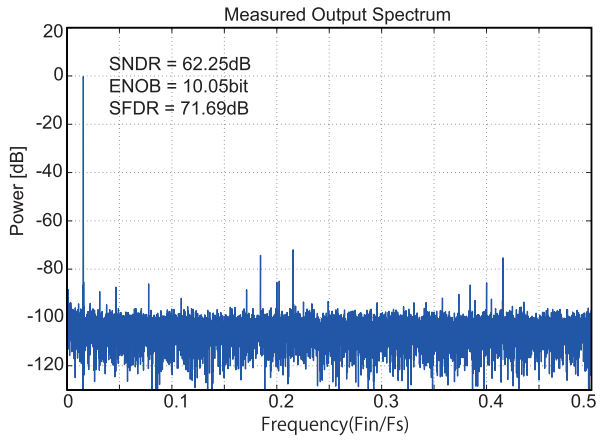

Fig. 9 Measured output power spectrum of cyclic ADC.

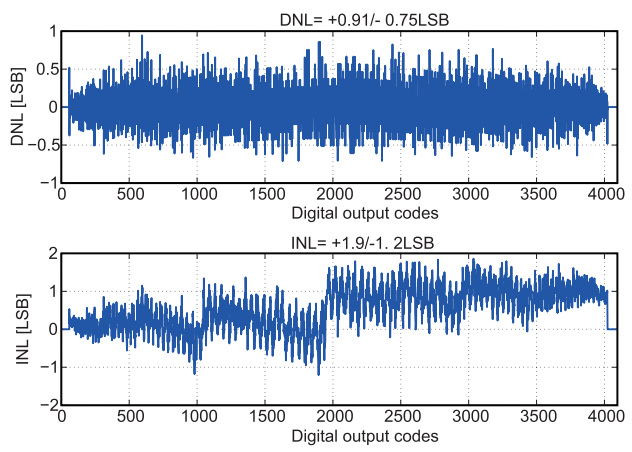

Fig. 10 Measured DNL and INL of cyclic ADC.

Table 2 Performance comparison.

Publication	[8]	[9]	[10]	[11]	[12]	[13]	[14]	[15]	This work
Technology(L,nm)	130	180	90	110	180	65	65	65	90
Area (mm^2)	0.5	1.43	0.097	0.079	1.98	0.26	0.55	0.073	0.037
Area(mm^2)/L(nm)^2	3.0E-05	4.4E-05	1.2E-05	6.5E-06	6.1E-05	6.2E-05	1.3E-04	1.7E-05	4.6E-06
Area Ratio	6.48	9.66	2.62	1.43	13.38	13.47	28.50	3.78	1.00
Architecture	Pipeline(TDC)	Pipeline	SAR	SAR	Pipeline	Pipeline	SAR	SAR	Cyclic
Supply Voltage(V)	1.3	1.6	1.2	0.9	1.2	1	1.2	1.1	1.4
Sampling Rate (MS/s)	70	60	50	1	20	200	80	95	1.25
Resolution (bits)	11	14	N/A	12	15	N/A	14	11	12
SNDR(dB)	69.3	76.9	71	68.3	75.9	65	71.3	63.1	62.3
ENOB (bit)	11.2	12.5	11.5	11.05	12.3	10.5	11.55	10.2	10.5
DNL (LSB)	0.71/-0.78	0.53/-0.51	N/A	0.28/-0.29	N/A	1	0.4/-0.4	0.70/-0.84	0.94/-0.71
INL (LSB)	0.53/-0.79	0.57/-0.60	N/A	0.55/-0.42	N/A	1.25	1.3/-1.3	0.79/-0.84	1.90/-1.20
Power(mW)	6.38	67.8	4.2	0.024	2.96	11.5	31.1	1.36	0.8
FoM(fJ/conv.step)	38.2	197.6	28.7	11.7	29	39.7	129.5	22	370.2

4. Conclusion

We have designed and fabricated a non-binary cyclic ADC with a radix-value self-estimation scheme in 90 nm CMOS technology. The redundancy of the proposed ADC tolerates the conversion errors caused by relaxed-accuracy devices and circuit components so that the circuit design can be greatly simplified. Measurement results demonstrate the validity of the proposed ADC architecture and the effectiveness of the proposed radix-value self-estimation scheme.

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